IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LINEAR TECHNOLOGY CORPORATION	)	
	)	
Plaintiff,	)	C.A. No. 06-476-GMS
	)	
v.	)	**PUBLIC VERSION**
	)	
MONOLITHIC POWER SYSTEMS, INC.	)	**JURY TRIAL DEMANDED**
	)	
Defendant.	)	
	)	

MONOLITHIC POWER SYSTEMS, INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Linear Technology Corporation ("Linear") is asserting two patents against Monolithic Power Systems, Inc. ("MPS") – U.S. Patent Nos. 5,481,178 ("the '178 patent") and 6,580,258 ("the '258 patent") (collectively, the "Linear Patents").

The asserted claims of the Linear Patents are directed at a voltage regulator that employs two ***distinct*** states of circuit operation: (1) a first state in which the output voltage is maintained at an essentially constant value by switching two transistors in complementary fashion through a first control signal generated by a duty cycle control circuit; and (2) a second state in which the output voltage is maintained at a different average value by disabling these two transistors through a second control signal generated by a "sleep mode" circuit. Thus, as reflected in the claim language, the specification, and the prosecution history, the Linear Patents contain specific limitations that the claimed voltage regulator: (1) transition from one mode of operation to the other at a fixed output current value; (2) be controlled by two distinct control signals, each of which is generated by a distinct circuit; and (3) maintain the output voltage at different average values depending upon which of the two modes of operation is being employed. In other words, the claimed states of operation are fundamentally different in terms of the output current and voltage levels and the control circuitry and signals involved. MPS's products do not operate in this fashion. Consequently, Linear has been forced to propose improper constructions that are aimed at conflating the two distinct states of circuit operation by ignoring claim limitations and reading out the claim language.

Linear alleges that one MPS product, identified as the MP1543, infringes claims 1, 34 and 41 of the '178 patent and claims 1 and 34 of the '258 patent. Linear has alleged that a second MPS product, identified as the MP18551, infringes claims 1, 2, 34, 41 and 55 of the '178 patent and claims 1, 2, 3 and 34 of the '258 patent. Since the MP18551 does not even have a state of circuit operation in which both switching transistors are simultaneously off, MPS is at a loss to understand why Linear would accuse that product. In any event, MPS has asked Linear to re-evaluate its position, which Linear appears to be doing.

Both of the Linear Patents have been the subject of previous lawsuits. All but one of those lawsuits resulted in settlements. The exception is the very recent (May 22, 2007) Initial Determination by Judge Sidney Harris of the United States International Trade Commission. *In re Certain Voltage Regulators*, 337-TA-564, Initial Determination (J.A. Tab Q).[1] Judge Harris construed various of the disputed claim terms and, based upon those constructions, concluded that the respondent in that case did not infringe any of the claims of the '258 patent asserted against it. Not surprisingly, Linear's proposed constructions in this case contradict those of Judge Harris. Furthermore, many of Linear's proposed constructions also differ from those adopted by Judge Fern Smith of the Northern District of California in *Linear Technology Corporation v. Impala Linear Corporation, et al.*, Case No. C 98-1727 (the "*Impala* Litigation"), which involved the '178 patent.[2] For the disputed terms at issue in this case, MPS's proposed constructions are consistent with those previously adopted by Judge Harris and Judge Smith.

II. THE RELEVANT TECHNOLOGY

A. Synchronous Switching Voltage Regulators – The Basics

Voltage regulators, including switching voltage regulators, have been in use for decades. They typically are used to convert an unregulated and variable input voltage (*e.g.*, from a battery) into a well-regulated output voltage – *i.e.*, a regulated voltage that is constrained to a predetermined and essentially constant value. As stated in the specification of the '178 patent, "[t]he purpose of a voltage regulator is to provide a predetermined and constant output voltage to

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[1] MPS and Linear have reached agreement as to various documents that will be included in the Joint Appendix ("J.A.") and have assigned letters to the tabs that will be used to identify the individual documents. Consistent with this Court's preference, the Joint Appendix will be filed on June 26, 2007, along with the answering claim construction briefs.

[2] The *Impala* Court issued a June 9, 1999, Claim Construction Order (J.A. Tab N). Following summary judgment, Linear appealed certain claim construction rulings to the Federal Circuit, which issued a published opinion on August 17, 2004. *Linear Technology Corp. v. Impala Linear Corp.*, 379 F.3d 1311 (Fed. Cir. 2004) (J.A. Tab P). After remand, the parties to the *Impala* Litigation settled.

a load from a poorly-specified and fluctuating input voltage source." '178 patent (J.A. Tab A), at 1:12-14.

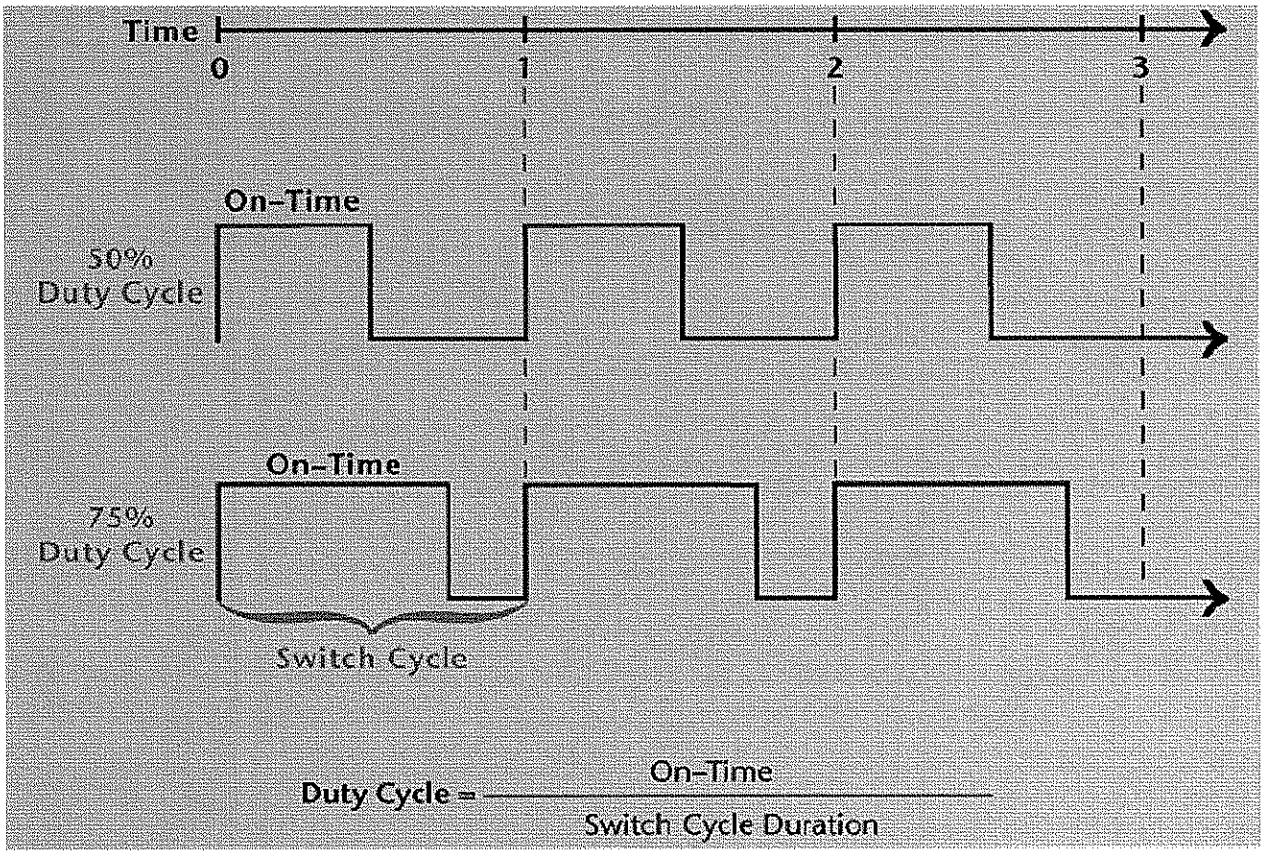
The electronic circuitry in devices such as cellular telephones requires an essentially constant voltage to operate. The telephone circuitry, for example, includes many thousand very small and delicate transistors designed to operate at a regulated voltage, *e.g.*, 1.8 volts. If that voltage level were to drop significantly below 1.8 volts, the transistors would stop functioning reliably. Conversely, if the voltage level were to rise substantially above 1.8 volts, the transistors could be damaged. The battery in a cellular telephone, however, will supply a varying voltage over time as the battery discharges and based upon the instantaneous demand for power. The purpose of a voltage regulator is to draw power from the battery at this potentially widely-varying voltage and to deliver that power to the telephone circuitry at a well-defined and regulated voltage.

There are different types of voltage regulators. One type is known as "switching" regulators. Within the class of switching regulators, there is a sub-class referred to as "synchronous switching" regulators. The term "synchronous" in this context indicates that the switching transistors are "driven out of phase to supply current at a regulated voltage to a load." '178 patent (J.A. Tab A), at 7:40-43. These regulators typically contain two transistors that rapidly switch "on" and "off" out of phase with each other. The switching of the transistors controls the flow of electric power from an unregulated voltage source (*e.g.*, a battery), through one of the two transistors to a set of feedback and filtering components that "regulate" the output voltage to a predetermined and essentially constant value. The filtering components commonly include an output inductor and capacitor. *See* '178 patent (J.A. Tab A), at 1:24-27 ("The switching regulator employs inductive energy storage elements to convert the switched current pulses into a steady load current."); 3:66-4:4. By controlling when and how each switching transistor is turned "on" and "off," it is possible to control the flow of energy from the input to the load, both in terms of the output voltage and the amount of energy transferred over time

(referred to as "power"). The regulated output voltage is then provided to a "load" (*e.g.*, chips in a cellular telephone) in order to power it. *See id.*

One well-established technique for regulating the output voltage in a switching voltage regulator is to adjust the turning "on" and "off" of the switches based on "feedback" information. "Feedback" generally refers to the use of information from one part of a system as input for another part of the same system, particularly for self-correcting, self-regulating or control purposes. Feedback and control circuits enable switching voltage regulators to regulate the output voltage in a changing environment. A drop in the battery voltage, for example, could cause a corresponding drop in the output voltage of a switching voltage regulator unless the operation of the switches is adjusted based upon feedback from the output voltage. If the feedback information indicates that the output voltage is below the regulated value, the switching voltage regulator will draw additional, or longer duration, pulses of power from the battery until the output voltage reaches the regulated value.

This response can be characterized in terms of a "duty cycle" (measured in percentages), which refers to the on-time of the switching transistor divided by the duration of an entire switch cycle. The term "switch cycle" refers to the sum of one "on-time" plus the corresponding "off-time" of a switching transistor. Higher duty cycles result in more energy being transferred through the voltage regulator to the load; lower duty cycles result in less energy being transferred, as illustrated in the following graphic:



There are two different methods for controlling the switching of the transistors that are relevant to the claim constructions in this case. The first scheme is called "pulse width modulation" ("PWM") and is the scheme used in the accused MPS products. In a PWM scheme, the switch cycle duration and thus the switch frequency are set to fixed values using a clock signal (*i.e.,* a regularly occurring signal used for timing purposes). While keeping these values constant, a PWM scheme adjusts the relative proportion between the "on-time" versus "off-time" of a switching transistor, as illustrated in the above graphic, while maintaining a constant switch cycle duration in order to vary the duty cycle (*i.e.,* the percentage of time that a switching transistor is "on" during a switch cycle).

The second scheme, which is described at length in the Linear Patents, is called "constant off-time" ("COT"). In a COT scheme, the off-time is held constant during each switch cycle, but the on-time of the switching transistor is varied in order to change the duty cycle. These changes in the "on-time" of a COT scheme cause corresponding changes in its switch cycle duration,

which is equal to the sum of the off-time (constant) and on-time (varying). In other words, if the on-time gets longer, and the off-time stays the same, the switching cycle will get longer. *See* '178 patent (J.A. Tab A), at 4:8-52, 6:16-33. In contrast, the switch cycle duration of a PWM scheme is set to a fixed value by a clock signal.

Although either a PWM or COT scheme can be utilized to vary the duty cycle of switching transistors, the particular scheme used has a fundamentally different impact on the design and operation of a voltage regulator that utilizes such transistors. Changes in input voltage in a PWM regulator (such as the accused MP1543) can affect the output current level at which both of the regulator's switching transistors are simultaneously off. In contrast, similar changes in input voltage for a COT regulator (such as those described in the Linear Patents) do ***not*** affect the output current level at which both of the switching transistors are simultaneously off. *See* '178 patent (J.A. Tab A), at 4:53-60.

B. The Linear Patents

Both Linear Patents derive from the same patent application. Thus, the specifications for these patents are essentially the same. The Linear Patents describe a synchronous switching voltage regulator that operates in one of two states.

In the first state of circuit operation, the regulator uses a feedback mechanism to control the duty cycle of a pair of synchronously switched transistors. *See* '178 patent (J.A. Tab A), at 6:16-33. In the second state, referred to as "sleep mode," both transistors are turned off, and energy previously stored in a capacitor is supplied to the load. *See* '178 patent (J.A. Tab A), at 6:34 – 7:21.

As explained above, the advantage of using a feedback loop to control the duty cycle of the switching transistors is the ability to tightly control the output voltage. The disadvantage is that the error amplifier and switch control components consume power that cannot be delivered to the load. At higher load currents, these losses are not significant. At low output currents, however, when the load is drawing very little power but the regulator's internal components are still operating and thus consuming power, the losses become relatively more significant.

The Linear patents describe the second state of circuit operation, or "sleep mode," as a solution to the problem of power loss at low output currents. The alleged invention of the Linear Patents is this "second state" of circuit operation, in which a specific type of feedback – based on ***monitoring the regulator's output current*** on the ***output side*** – is used to turn off the switching of both transistors at a fixed output current level.

Figure 2 depicts the voltage regulator of Figure 1 with additional circuitry for the claimed sleep mode:

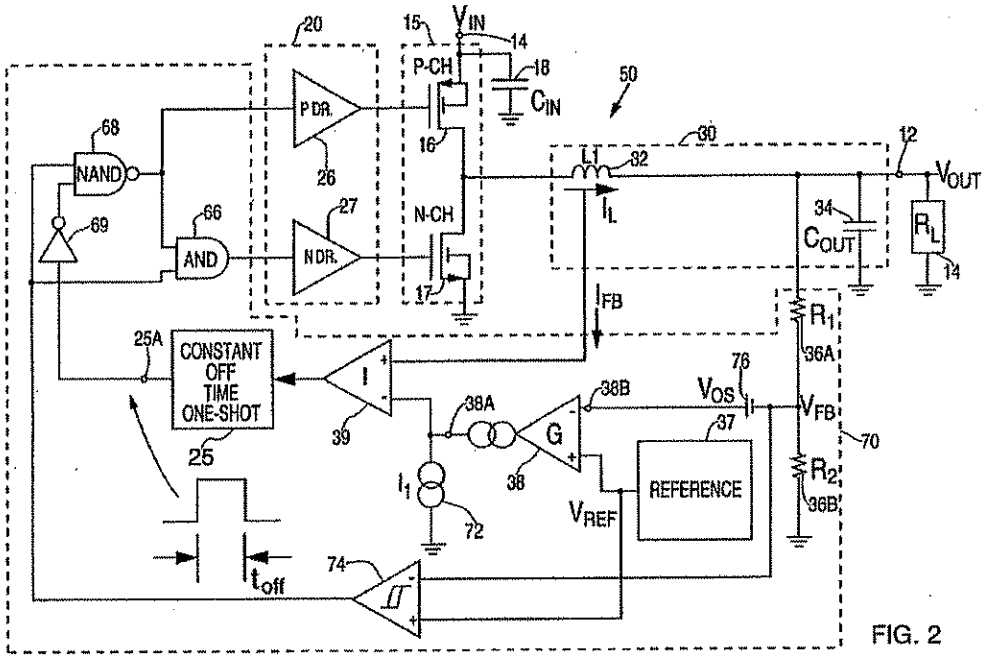


FIG. 2

According to the '178 patent, "[a]t high load current levels (e.g., greater than 20 percent of the maximum rated output current) control circuit 70 operates similar to control circuit 35 of FIG. 1." '178 patent (J.A. Tab A), at 6:17-19. In other words, at high load currents, the circuit will monitor the feedback voltage (actually a version of the feedback voltage offset by the incremental voltage V_{OS}) using the error amplifier 38. The circuit uses the output of the error amplifier 38, comparator 39, and COT one-shot 25 to adjust the duty cycle to keep the output voltage tightly regulated. These components constitute the "duty cycle control" circuitry, which operates in connection with the first state of circuit operation.

Figure 2 also includes additional circuitry to monitor the load current and shut down both switching transistors for a period of time when the load current drops below a specified level. In very general terms, this control scheme operates by monitoring the output current – the current that the regulator is supplying to the load. The patents teach that if the monitored output current falls below a threshold level of the maximum rated output current – for example, below 20% of a maximum rated output current of 1 amp – then a single control signal is used to turn "off" both of the switching transistors. Specifically, Figure 2 shows a hysteretic comparator 74 that compares the feedback voltage V_{FB} to the reference voltage V_{REF}. *See* '178 patent (J.A. Tab A), at 6:36-41. A hysteretic comparator is a comparator that only responds if the difference between V_{FB} and V_{REF} is large enough. *Id.* When the load current (as represented by feedback current I_{FB}) is below the specified threshold level, constant current source I_1 is used to force the comparator 39 and one-shot 25 to increase the duty cycle of the switching transistor beyond what is necessary to maintain the regulated voltage. *Id.* at 6:41-44. This results in the output voltage rising above the regulated voltage until the feedback voltage V_{FB} reaches a level higher than that corresponding to the regulated output voltage and sufficiently high to trigger the hysteretic comparator 74. As stated in the patent, "[t]his over voltage condition is intentionally induced at low average output currents. . . ." *Id.* at 6:41-42. The comparator then outputs a signal to turn off both switching transistors. *Id.* at 6:44-46. In this way, components V_{OS} (the offset voltage) and I_1 (a constant current source) are used to ensure that the regulator is in only one state at a time. *Id.* at 6:21-25, 41-44. Specifically, these components are used to provide an output voltage for the claimed second state (*i.e.*, "sleep mode") that has a different average value than the regulated output voltage for the first state. *Id.* at 6:21-25, 61-64. These components constitute the "sleep mode" circuitry, which operates in connection with the second state of circuit operation.

III. CLAIM CONSTRUCTION PRINCIPLES

"'Claim construction' is the judicial statement of what is and is not covered by the technical terms and other words of the patent claims." *Netword, LLC v. Centraal Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001). Just like the interpretation of statutes, claim construction is a question of law to be resolved by the court. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995).

The Federal Circuit has "frequently stated that the words of a claim 'are generally given their ordinary and customary meaning'" and has "made clear, moreover, that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc). "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification," which the Federal Circuit has counseled is usually "the single best guide to the meaning of a disputed term." *Id.* at 1313, 1315. The prosecution history of the claims is also a useful guide in construing claims, as "the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.* at 1317. Likewise, "[d]ictionaries or comparable sources are often useful to assist in understanding the commonly understood meaning of words and have been used both by our court and the Supreme Court in claim interpretation." *Id.* at 1322.

IV. CLAIM CONSTRUCTIONS FOR THE ASSERTED CLAIMS

A. "threshold" / "a threshold fraction of maximum rated output current for the regulator" / "selected sleep mode current level"

Claim Term	MPS Construction	Linear Construction
threshold	a fixed point, such as a current of voltage level, for a given effect, result or response	predetermined level or value at which some change in circuit operation takes place ("predetermined" means determined by design, and included levels or values that may be fixed or variable)
a threshold fraction of maximum rated output current for the regulator	a fixed number greater than zero that is selected as a proportionality of two numbers, the proportion being relative to maximum rated output current	a predetermined level or value at which some change in circuit operation takes place, wherein that level or value is a number greater than zero that represents the proportionality of two positive numbers, the proportion being relative to a rated maximum output current ("predetermined" means determined by design, and includes levels or values that may be fixed or variable.).
selected sleep mode current level	a fixed current level that represents a percentage of maximum rated output current below which the regulator is operated in a second mode of circuit operation	a current level below which the regulator enters into a second mode of operation

1. Overview

The asserted claims are directed to the concept of turning the two switching transistors "off" for a period of time by monitoring the output current and comparing it to a selected threshold value. The '178 patent claims explicitly require that both switching transistors be turned "off" when the output current falls below the selected threshold value, alternately

described as "a threshold fraction of maximum rated output current for the regulator" (claims 1, 34 and 41)[3] or as a "selected sleep mode current level" (claim 55):

'178 Patent Claim	Claim Language
Claims 1, 34	"both switching transistors to be simultaneously OFF for a period of time if a sensed condition of the regulator indicates that the current supplied to the load falls below a ***threshold fraction of maximum rated output current for the regulator***"
Claim 41	"both switching transistors to be simultaneously OFF for a period of time when the current supplied to the load falls below a ***threshold fraction of maximum rated output current for the regulator***"
Claim 55	"prevents the drive circuitry from turning on either of the pair of synchronously switched switching transistors if the feedback information indicates that the current supplied to the load by the regulator falls below ***selected sleep mode current level***"

At the appropriate time, MPS anticipates filing a motion for summary judgment establishing that the accused MP1543 does not operate in this manner. In the MP1543, there is no selected output current threshold value below which both switching transistors are turned "off." The point relative to the output current at which the regulator transitions to having both switching transistors "off" fluctuates substantially with changes in the input voltage and, in any event, is not determined by sensing output current.

To avoid this result, Linear has proposed constructions for the claim terms "threshold," "a threshold fraction of maximum rated output current for the regulator," and "selected sleep mode current level" that, if adopted, would render those limitations meaningless. In particular, Linear proposes that the claimed "threshold," "threshold fraction," and "selected current level" are not fixed or selected at all but rather are allowed to fluctuate arbitrarily without limit. Under Linear's interpretation, these claim limitations would be rendered meaningless, since any regulator having a period of time when both switching transistors are "off" would necessarily

[3] Voltage regulators are marketed with a maximum rated output current. For example, the maximum rated output current for the accused MP1543 part is 1 amp.

enter that period of time at some arbitrary output current level, which would represent a fluctuating fraction of the maximum rated output current. Stated differently, if the claimed fraction is allowed to fluctuate arbitrarily without limit (and Linear offers none), it is no limitation at all. A person of ordinary skill in the art would understand that the "threshold fraction" of the "maximum rated output current" is a fixed number, as recognized by the *Impala* court. This is confirmed both by examining the claims, specification and file history and by considering the definitions of "threshold" set forth in technical dictionaries.

2. The "Threshold" Terms Should Be Construed In Accordance With Their Ordinary Meaning.

The Federal Circuit has "frequently stated that the words of a claim 'are generally given their ordinary and customary meaning'" and that " the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention . . . ." *Phillips,* 415 F.3d at 1312-13. The term "threshold" is a well-understood term to electrical engineers, and simply means a fixed point, such as a current of voltage level, that is selected by a design engineer or another circuit for a given effect, result or response. "Dictionaries or comparable sources are often useful to assist in understanding the commonly understood meaning of words and have been used both by our court and the Supreme Court in claim interpretation." *Id.* at 1323. For example, Gibilisco, Illustrated Dictionary of Electronics, 8th ed. (2001) (J.A. Tab S), defines ***threshold*** as "2. A predetermined point, such as of minimum current or voltage, for the start of operation of a circuit or device." Likewise, Wiley Electrical and Electronics Engineering Dictionary (2004) (J.A. Tab U) defines ***threshold*** as "[t]he point, level or value of a quantity which must be exceeded to have a given effect, result, or response, such as detection, activation, or operation."

Similarly, a person of ordinary skill in the art would understand that the reference in claim 55 to a "selected sleep mode current level" is intended to refer to a fixed output current value "selected" or "chosen" by a design engineer or another circuit, not an unspecified, fluctuating current level. "Selected" is also a commonly understood term. "In some cases, the

ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words. In such circumstances, general purpose dictionaries may be helpful." *Phillips,* 415 F.3d at 1314. Here, for example, the American Heritage College Dictionary, Third Edition (1993) (J.A. Tab R), defines ***select*** as "to take as a choice from among several; pick out."

These dictionary definitions provide unbiased evidence of the well-understood meanings of commonly used terms, and clearly support MPS's proposed constructions, as contrasted with Linear's unsupported, litigation-inspired constructions. *Phillips,* 415 F.3d at 1323.

Indeed, the District Court in the *Impala* Litigation largely agreed with the ordinary meaning of the term "threshold fraction" and construed it to mean "a number greater than zero that represents the proportionality of two numbers, the proportion being relative to a rated maximum output current." June 9, 1999, Claim Construction Order (J.A. Tab N) at 12. Importantly, the District Court specifically rejected Linear's argument that the "threshold fraction" could be variable, reasoning that "***[b]ecause the maximum rated output is constant, the Court has difficulty discerning how the threshold fraction of that output could be anything other than a constant percentage***." *Id.* at 13 (emphasis added). Linear did not appeal that construction to the Federal Circuit.

3. The Only Discussion In The Specification Concerning The Transition From High Output Current To Low Output Current Refers To A Fixed Value

The specification confirms that the terms "threshold fraction" and "selected sleep mode current level" are used in accordance with their widely understood ordinary meanings. The specification does not use or define the phrase "threshold fraction" or "selected sleep mode current level." However, consistent with the ordinary usage of "threshold" and "selected," the only discussion in the specification concerning the transition point into "sleep mode" refers to a fixed value, *i.e.*, "20 percent of the maximum rated output current." For example:

- The '178 specification introduces the concept of "sleep mode" in column 5: "As will be discussed in greater detail below, constant current source I_1 72 and comparator 74 allow push-pull switch 15 to go into ***a state of operation where both MOSFETS 16 and 17 are simultaneously OFF*** under conditions where the output voltage V_{OUT} can be maintained substantially at the regulated voltage V_{REG} by output capacitor C_{OUT}. This state of operation is referred to herein as a "***sleep mode***." '178 patent (J.A. Tab A) at 5:59-66 (emphasis added).

- In the next column, the '178 specification describes "high load current levels" as exceeding a threshold fraction of the maximum rated output current: "At ***high load current*** levels (e.g., greater than ***20 percent of the maximum rated output current***) control circuit 70 operates similar to control circuit 35 of FIG. 1." '178 patent (J.A. Tab A) at 6:17-21 (emphasis added).

- Further down in the same column, the '178 specification describes the "invention" as selecting the current level for sleep mode to correspond with "low output current levels," *i.e.,* below the same threshold fraction of the maximum rated output current: "In accordance with the ***present invention***, regulator circuit 50 goes into ***sleep mode at low output current levels*** . . ." '178 patent (J.A. Tab A) at 6:34-36 (emphasis added).

This intrinsic description provides further support for the conclusion that the disputed terms are intended to have their ordinary meaning and refer to a fixed, selected output current value. There is no support in the specification for a construction of "a threshold fraction of maximum rated output current" or "selected sleep mode current level" that would encompass a broad range of output current values that fluctuate arbitrarily over time as, for example, the input source battery discharges and the input voltage to the regulator fluctuates. "In light of the statutory directive that the inventor provide a 'full' and 'exact' description of the claimed invention, the specification necessarily informs the proper construction of the claims." *Phillips*, 415 F.3d at 1316.

4. The Prosecution History Confirms That The Applicants Were Using The Terms To Refer To A Fixed Value

The prosecution history provides further confirmation that the claim terms "a threshold fraction of maximum rated output current for the regulator" and "selected sleep mode current level" are intended to have their ordinary meaning and refer to a fixed value. Those two terms were added to the '178 patent claims on June 5, 1995, in response to prior art rejections by the

PTO. Linear stated that it was amending its claims in order "to more particularly point out and distinctly claim that the switching transistors of applicants' regulator are turned off if the current supplied to the load falls below a threshold level," "i.e., below some fraction (*e.g.*, 20%) of the regulator's maximum rated output current." '178 patent prosecution history: June 5, 1995, Response (J.A. Tab K) at 6-7 (emphasis in the original).

Consistent with these statements, Linear amended each of the pending independent "two transistors off" claims to incorporate the express limitation that both switching transistors are turned "off" "***if a sensed condition of the regulator indicates that the current supplied to the load falls below a threshold fraction of the maximum rated output current for the regulator***,"[4] thereby surrendering the scope of the previously pending claims. *See* '178 patent prosecution history: June 5, 1995, Response (J.A. Tab K) at 1-5 (emphasis added). Moreover, Linear relied upon this limitation to distinguish a prior art reference (Josephson) cited by the Examiner: "Josephson teaches current limiting to turn off switching transistors to protect them from overcurrents . . . . Conversely, the synchronous switching regulator of the applicants' invention changes operating state ***under low output current conditions***, the precise opposite of the conditions which motivate the desire to turn off the transistors in Josephson's circuit." '178 patent prosecution history: June 5, 1995, Response (J.A. Tab K) at 8 (emphasis added).

"[A]rguments made during the prosecution history are relevant in determining the meaning of the terms at issue." *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1438 (Fed. Cir. 1988). *See also Alpex Computer Corp. v. Nintendo Co. Ltd.*, 102 F.3d 1214, 1221 (Fed. Cir. 1996) (same). When Linear was seeking to have the PTO issue the '178 patent, Linear described the "threshold fraction of maximum rated output current for the regulator" and "selected sleep mode current level" as a particular output current level, and gave "20%" as the example. This is in direct contrast to the arbitrary range of fluctuating output

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[4] This same limitation was stated using slightly different wording in application claim 97, which corresponds to issued claim 55: "the current supplied to the regulator falls below a selected sleep mode current level."

current levels that Linear now advances. Thus, the prosecution history provides further evidence that the terms are properly construed to mean a selected and fixed level of output current, below which the regulator enters into what Linear terms "sleep mode."

5. The Prosecution History Confirms That Linear Used The Terms "Threshold Fraction Of Maximum Rated Output Current" And "Selected Sleep Mode Current Level" Interchangeably

Furthermore, the prosecution history shows that Linear treated both terms as describing the same claim limitation. The claim that issued as claim 55 (reciting "selected sleep mode current level") was prosecuted as application claim number 97. '178 patent prosecution history: June 5, 1995, Response (J.A. Tab K) at 4-5. The claims that issued as independent claims 1, 34, 41 and 57 (reciting "threshold fraction of the maximum rated output current") were prosecuted as application claim numbers 1, 66, 80, and 99, respectively. *Id.* at 1-5. Linear's patent counsel addressed the examiner's prior art rejections by amending all five of these independent claims and stating for the record: "applicants have amended claims 1, 66, 80, ***97*** and 99 to more particularly point out and distinctly claim that ***the switching transistors of applicants' regulator are turned "off" if the current supplied to the load falls below a threshold level.***" *Id.* at 6-7 (emphasis added). Thus, the prosecuting attorney represented to the PTO that claim 55 [application claim 97] was being amended for the same purpose as claims 1, 34, 41 and 57 [application claims 1, 66, 80 and 99, respectively] – *i.e.*, to more particularly point out that these claims require a selected threshold level below which the switching transistors of the claimed regulator are turned "off."

In sum, during prosecution, Linear properly treated these two phrases as describing one and the same claim limitation, which is a fixed output current level that is selected for transitioning into "sleep mode." It is irrelevant whether that selected threshold is expressed as "a fraction of maximum rated output current" (*e.g.*, "20% of the maximum rated output current of 1 amp") or as a "selected sleep mode current level" (e.g., "200 milliamps"). Both expressions are equivalent.

6. Conclusion

For each of these reasons, there is no support for Linear's attempt to redraft its patent claims in order to remove the "threshold fraction" and "selected . . . level" limitations. The claims, the relevant dictionary definitions, the specification, the prosecution history, and a prior court decision all demonstrate that MPS's constructions are correct.

B. "first state of circuit operation" / "second state of circuit operation"

Claim term	MPS Construction	Linear Construction
first state of circuit operation	a state in which the output voltage is maintained during high load current conditions by switching the switching transistors in a complementary manner to provide power to the load	a state in which the switching transistors are both enabled for switching and are synchronously switched such that one transistor is ON and the other is OFF, with a varying duty cycle to maintain a regulated voltage at the output terminal.
second state of circuit operation	a state in which, as a result of low load current conditions, the output capacitor maintains the output voltage substantially at the regulated voltage, while the switching transistors are disabled	a state (excluding deadtime) during which both switching transistors are OFF and current is supplied to the load by the output capacitor.

MPS's construction of the first and second states of circuit operation is straightforward: the first state of circuit operation is the behavior of the claimed regulator during ***high*** load current, and the second state of circuit operation is the behavior of the claimed regulator during ***low*** load current. This distinction based on load current conditions is fully supported by the intrinsic evidence, as confirmed by Judge Harris in construing these terms for the '258 patent in the recent *Voltage Regulators* ITC case.

As Judge Harris found, [redacted]." *In re Certain Voltage Regulators*, 337-TA-564, Initial Determination (J.A. Tab Q), at 24-25 (finding that "[redacted]

[redacted].”). This is true for all relevant embodiments disclosed in the specification. *See, e.g.,* ’178 patent (J.A. Tab A), Figure 2 and 7. The specification clearly describes the first state of circuit operation as occurring during high load current conditions:

> ***At high load current levels*** (e.g., greater than 20 percent of the maximum rated output current) control circuit 70 operates similar to control circuit 35 of FIG. 1. In FIG. 2, the current feedback I_{FB} is again provided to the non-inverting input of current comparator 39. Offset V_{OS} 76, which preferably is built into amplifier 38, level-shifts feedback voltage V_{FB} slightly below reference voltage V_{REF}, thus keeping the output of hysteretic comparator 74 high during high current conditions. When the feedback current I_{FB} exceeds the current supplied to the inverting input of current comparator 39, the output of comparator 39 goes HIGH so as to initiate the switch “OFF” cycle.
>
> During the “OFF” cycle, output 25A of one-shot circuit 25 is HIGH, which turns P-MOSFET 16 OFF and N-MOSFET 17 ON. After a constant time set by one-shot circuit 25, output 25A goes LOW, thus initiating the next “ON” cycle where P-MOSFET 16 ON and N-MOSFET 17 OFF.

’178 patent (J.A. Tab A), at 6:17-33 (emphasis added). In other words, at high load current levels, the output voltage is maintained by switching the switching transistors (16 and 17) in a complementary manner (*i.e.,* first, P-MOSFET 16 OFF and N-MOSFET 17 ON, and then P-MOSFET 16 ON and N-MOSFET 17 OFF) to provide power to the load.

Likewise, the specification clearly describes the second state of circuit operation as occurring during low load current conditions:

> In accordance with the present invention, regulator circuit 50 goes into ***sleep mode at low output current levels*** as follows. Hysteretic comparator 74 monitors the feedback voltage V_{FB} and goes LOW when V_{FB} exceeds a predetermined voltage value in excess of the reference voltage V_{REF}. Such a condition is indicative of the output voltage V_{OUT} exceeding a predetermined voltage value in excess of the regulated voltage V_{REG}. This over voltage condition is intentionally induced at low average output currents by providing a constant current source I_1 72 coupled in parallel with amplifier 38. During the over voltage condition both MOSFETS 16 and 17 are maintained OFF by way of AND gate 66 and NAND gate 68.
>
> . . .
>
> In the above-described state of operation (i.e., “***sleep mode***”) where MOSFETs 16 and 17 are both simultaneously OFF, the output load 14 is supported ***substantially*** by output capacitor C_{OUT}.

'178 patent (J.A. Tab A), at 6:34-47, 61-64 (emphasis added). In other words, at low load current levels, the output capacitor (C_{OUT}) maintains the output voltage substantially at the regulated voltage, while the switching transistors are disabled (*i.e.,* MOSFETs 16 and 17 are both simultaneously OFF).

Thus, as framed by Judge Harris, "[redacted]. *In re Certain Voltage Regulators*, 337-TA-564, Initial Determination (J.A. Tab Q), at 24. Judge Harris correctly concluded that [redacted]. *Id.*

The prosecution history, moreover, unequivocally demonstrates that Linear restricted its claimed invention to embodiments in which the first and second states of circuit operation are linked to the load current level and disclaimed other possible embodiments in order to overcome prior art rejections. During prosecution of the parent '178 patent, the Examiner initially rejected Linear's claims over the prior art Inam patent. *See* '178 patent prosecution history: April 7, 1994, Office Action (J.A. Tab F) at 2. In response, Linear amended its claims "to more particularly point out that the invention is based on turning off both switching transistors as a ***function of the load current***." '178 patent prosecution history: July 15, 1994, Response (J.A. Tab G) at 13 (emphasis added). In so doing, Linear explained that "Applicants' invention is a switching voltage regulator control circuit having improved efficiency ***during periods of low load current***." *Id.* at 12 (emphasis added). Moreover, Linear explicitly stated that this distinction was necessary to distinguish Linear's claims from the prior art Inam patent: "there is no teaching in Inam that the circuit turns off both transistors 208 and 212 as a ***function of the load current***." *Id.* at 14 (emphasis added).

Linear repeatedly relied on this load current level distinction in response to subsequent office actions. In particular, in a December 5, 1994, office action, the Examiner rejected the revised claims as obvious over Inam and the Josephson patent "which shuts off transistors in

response to a predetermined threshold." '178 patent prosecution history: Dec. 5, 1994, Office Action (J.A. Tab J) at iii. In response, Linear once again "amended . . . to more particularly point out and distinctly claim that the switching transistors of applicants' regulator are turned off if the current supplied to the load falls below a threshold level." '178 patent prosecution history: June 5, 1995, Response (J.A. Tab K) at 6-7 (emphasis in original). Linear explained that

> ***Applicants' invention*** is directed to maintaining high efficiency in a switching voltage regulator circuit by providing ***two states of circuit operation***. At ***high load current levels***, the circuit provides a regulated DC output voltage by alternatively turning on and off the two transistors of a push-pull switch. When the ***output current of the regulator drops below a threshold level*** – i.e. below some fraction (e.g., 20%) of the regulator's maximum rated output current – the regulator's switching transistors are turned off simultaneously for a period of time while previously stored energy in the regulator's output circuit supplies current to the load.

Id. at 6 (emphasis added).

These repeated disclaimers – made by Linear during prosecution in order to overcome prior art rejections – wholly support linking the first state of circuit operation to high load current and the second state of circuit operation to low load current, as proposed by MPS and as construed by Judge Harris in the International Trade Commission. "The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution." *Chimie v. PPG Indus.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (internal quotation marks omitted); *accord Andersen Corp. v. Fiber Composites, LLC,* 474 F.3d 1361, 1374 (Fed. Cir. 2007) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well.").

Claims 1 and 34 of the later filed '258 patent are nearly identical to the claims originally rejected during the prosecution of the '178 patent. They recite the same first and second states of circuit operation. Moreover, the '258 patent contains the same specification as, and claims priority to, the '178 patent. The Federal Circuit has made clear that "[w]hen multiple patents derive from the same initial application, the ***prosecution history regarding a claim limitation in***

any patent that has issued applies with equal force to subsequently issued patents that contain the same claim limitation." *Elkay Manufacturing Co. v. Ebco Manufacturing Co.*, 192 F.3d 973, 980 (Fed. Cir. 1999) (emphasis added). Such disclaimer cannot be recaptured through claim construction. *Hakim v. Cannon Avent Grp., PLC*, 479 F.3d 1313, 1317 (Fed. Cir. 2007). Moreover, "although a disclaimer made during prosecution can be rescinded, permitting recapture of the disclaimed scope, the prosecution history must be sufficiently clear to inform the examiner that the previous disclaimer, and the prior art that it was made to avoid, may need to be re-visited." *Id.* at 1318. *See also Alloc, Inc. v. United States Int'l Trade Comm'n*, 342 F.3d 1361, 1372 (Fed. Cir. 2003) (because the subject matter was "expressly disavowed" "during prosecution of the parent," "the independent claims of the [child] patents incorporate the same limitations adopted by the applicant to secure allowance of the parent.").

During the prosecution of the '258 patent, Linear never expressed any intention or desire to rescind its prior disclaimers. Accordingly, the "first state of circuit operation" and the "second state of circuit operation" should be construed as proposed by MPS for both the '178 and '258 patents.

C. "first control signal" / "second control signal" / "third circuit"

Claim term	MPS Construction	Linear Construction
first control signal	a signal generated by the second circuit and used to affect the operation of other circuitry, which signal is separate and distinct from the "second control signal."	a control signal generated by the second circuit and used to affect the operation of other circuitry.
second control signal	a signal generated by the third circuit and used to affect the operation of other circuitry, which signal is separate and distinct from the "first control signal."	a control signal generated by the third circuit and used to affect the operation of other circuitry.

Claim term	MPS Construction	Linear Construction
third circuit	a circuit that is separate and distinct from both the "first circuit" and the "second circuit"	an assembly of electronic components forming a control circuit that is distinct from each of the first and second circuits in that not every electronic component of the circuits is the same

MPS and Linear agree that the "first control signal" is generated by the "second circuit" and used to affect the operation of other circuitry. Likewise, the parties agree that the "second control signal" is generated by the "third circuit" and used to affect the operation of other circuitry. The only dispute with regard to the two control signals is whether the "first control signal" and "second control signal" are separate and distinct. Likewise, with regard to the "third circuit," the dispute is whether that circuit must be separate and distinct from both the "first circuit" and the "second circuit."

According to the plain meaning of the claims, as well as the specification, the first and second control signals are separate and distinct. Linear's proposed constructions, on the other hand, improperly conflate these two signals into one, effectively reading one of the limitations out of the claims. *See Glaxo, Inc. v. Novopharm, Ltd.*, 110 F.3d 1562, 1566 (Fed. Cir. 1997) ("It is elementary patent law that all limitations are material."). "Because the patentee is required to 'define precisely what his invention is,' the [Supreme] Court explained, it is 'unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its terms.'" *Phillips*, 415 F.3d at 1312, quoting *White v. Dunbar*, 119 U.S. 47 (1886).

In the Linear Patents, the plain import of separately calling out a first control signal and a second control signal is that those control signals are distinct from one another. Indeed, the Federal Circuit has recognized the use of the "first" and "second" designators to indicate such a distinction. *See Bell Atlantic Network Services, Inc. v. Covad Communications Group, Inc.*, 262 F.3d. 1258, 1271 (Fed. Cir. 2001) (emphasis added):

> When describing the microprocessor that controls the transceivers, the specification states that "the variable transmission rates are controlled by a ***first***

> [program] and the mode of the transceiver is controlled by a ***second*** [program]." '786 patent, col. 11, ll. 35-39 (emphasis added). Thus, the "mode" and "rate" of the transceiver are controlled by ***separate*** programs.

See also Hynix Semiconductor, Inc. v. Rambus, Inc., No. CV-00-20905, 2004 U.S. Dist. LEXIS 23230, at *65-66 (N.D. Cal. 2004) (attached hereto as Ex. A) (construing "first external clock" and "second external clock" to require "different" timing information). For the same reasons, the plain import of calling out the third circuit separately from both the first circuit and the second circuit is that the third circuit is separate and distinct from the other two circuits.

"[T]he context in which a term is used in the asserted claim can be highly instructive." *Phillips,* 415 F.3d at 1314. Here, the first and second control signals are recited in separate claim limitations, and are used for different purposes. For example, the first control signal is "responsive to the first feedback signal" and used "to vary the duty cycle of the switching transistors to maintain the output terminal at the regulated voltage," while the second control signal is used "to cause both switching transistors to be simultaneously OFF for a period of time . . ." '178 patent (J.A. Tab A), claim 1. If the first and second control signals were indeed one and the same, as Linear would have it, there would have been no sensible reason to call them out separately. *See Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 93 F.3d 1572, 1579 (Fed. Cir. 1996):

> If the terms "pusher assembly" and "pusher bar" described a single element, one would expect the claim to consistently refer to this element as either a "pusher bar" or a "pusher assembly," but not both, especially not within the same clause. Therefore, in our view, the plain meaning of the claim will not bear a reading that "pusher assembly" and "pusher bar" are synonyms.

Accordingly, the natural reading of the claims dictates that the first and second control signals are separate and distinct. Likewise, if the third circuit were the same as either the first or second circuits, there would have been no reason to call it out separately.

The *Impala* court's constructions for these terms were consistent with MPS's constructions. In particular, the *Impala* court construed the "second circuit" as "a circuit that is distinct from each of the first and third circuit" and the "third circuit" as "distinct from each of

the first and second circuits." June 9, 1999, Claim Construction Order (J.A. Tab N), at 8-9. Likewise, it construed "control signal" as "a signal generated by a circuit and used to affect the operation of other circuitry." *Id.* at 8. Since, according to the plain language of the claims, the first control signal is generated by the second circuit and the second control signal is generated by the "distinct" third circuit, the first and second control signals must be distinct. Linear appealed certain aspects of the *Impala* court's constructions, but did not appeal these points.

The specification also confirms that the first and second control signals are separate, and are generated by separate second and third circuits. In particular, the specification describes the first control signal (*e.g.*, 25A in Figure 2) as being generated by the constant off-time one-shot circuitry: "When the feedback current I_{FB} exceeds the current supplied to the inverting input of current comparator 39, the output of comparator 39 goes HIGH so as to initiate the switch 'OFF' cycle. During the 'OFF' cycle, output 25A of one-shot circuit 25 is HIGH, which turns P-MOSFET 16 OFF and N-MOSFET 17 ON. After a constant time set by one-shot circuit 25, output 25A goes LOW, thus initiating the next 'ON' cycle where P-MOSFET 16 ON and N-MOSFET 17 OFF." '178 patent (J.A. Tab A), at 6:25-33.

In contrast, the specification describes the second control signal (*e.g.*, output of 74 in Figure 2) as being generated by the comparator 74:

> As a result, V_{OUT} will begin to increase beyond the regulated voltage V_{REG}, causing the feedback voltage V_{FB} to trip hysteretic comparator 74 at a predetermined voltage value in excess of V_{REF}. When comparator 74 trips, its output goes LOW to turn both MOSFET 16 and 17 OFF to put the regulator circuit into sleep mode.

'178 patent (J.A. Tab A), at 6:55-60. This distinction is illustrated in Figure 2 (annotated) of the '178 patent:

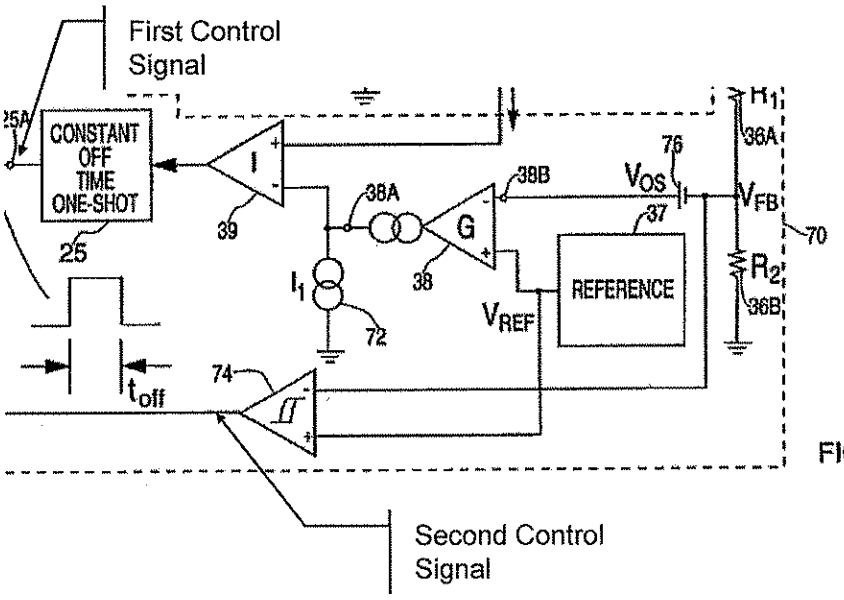


FIG. 2

Thus, the specification reinforces the plain language of the claims, making clear that the first and second control signals are separate and distinct from one another, and that the third circuit is separate and distinct from the first and second circuits.

D. "regulated voltage" / "substantially at the regulated voltage"

Claim Term	MPS Construction	Linear Construction
regulated voltage	a predetermined and essentially constant output voltage	A voltage having a controlled value
substantially at the regulated voltage	a voltage that has a different average value than the regulated voltage	A voltage having a controlled value, and allowing for, but not requiring, greater variation than the regulated voltage (*i.e.*, controlled value).

The '178 patent specification states that "[t]he purpose of a voltage regulator is to provide a predetermined and constant output voltage to a load from a poorly-specified and fluctuating input voltage source." '178 patent (J.A. Tab A), at 1:12-14. Thus, the specification clearly expresses the commonly understood construction of "regulated voltage" – it is a voltage that is predetermined and essentially constant. For example, Wiley Electrical and Electronics Engineering Dictionary (2004) (J.A. Tab U) defines ***regulate*** as "3. [t]o maintain a voltage,

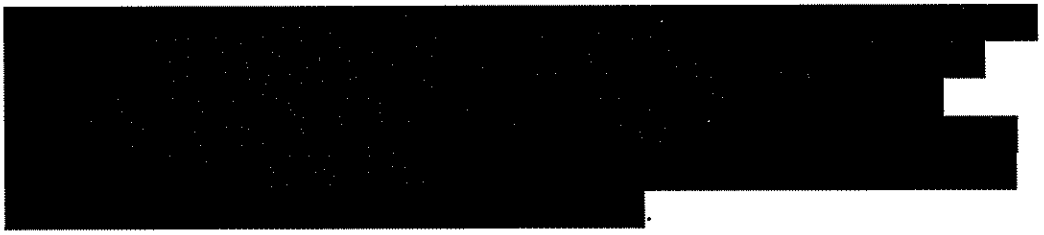
current, or the like, within specified values" and ***regulated power supply*** as "[a] power supply that has circuitry to maintain the output voltage constant when the input line or load varies." Likewise, Gibilisco, Illustrated Dictionary of Electronics, 8th ed. (2001) (J.A. Tab S) defines ***regulator*** as "1. [a] device that automatically holds a quantity to a constant value (e.g., a voltage regulator)" and ***regulated power supply*** as "[a] power supply whose output is held automatically to a constant level or within a narrow range, regardless of loading variations."

The Linear Patent claims use the claim limitations "regulated voltage" and "substantially at the regulated voltage" to describe different aspects of the alleged invention that occur during different states of circuit operation. The "regulated voltage" limitation is used to describe the regulated output voltage of the claimed voltage regulator when the regulator is in its "first state" of operation. *See, e.g.,* '178 patent (J.A. Tab A), claim 1 (during first state, first control signal used "to maintain the output terminal ***at the regulated voltage***"); claim 41 ("to maintain the output terminal ***at the regulated voltage*** during a first state of circuit operation"); '258 patent (J.A. Tab B), claim 1 ("during a first state of circuit operation . . first control signal . . . maintain[s] the output ***at the regulated voltage***") (emphasis added).

In contrast, the "substantially at the regulated voltage" limitation is used to describe a different output voltage of the claimed voltage regulator when the regulator is in its distinct "second state" of operation. *See, e.g.,* '178 patent (J.A. Tab A), claim 41(c) ("a second state of circuit operation . . . so as to allow the output capacitor to maintain the output ***substantially at the regulated voltage***"); '258 patent (J.A. Tab B), claim 1 ("a second state of circuit operation. . . during which the output capacitor maintains the output ***substantially at the regulated voltage***") (emphasis added).

The two claim limitations cannot mean the same thing. [redacted], the patent specification makes clear that a voltage "substantially at the regulated voltage" must have a different average value than the regulated value. Indeed, the voltage regulators disclosed in the Linear Patents would not work if the two voltages had the same average value. As described above in connection with the "first state" / "second state" and "first control signal" / "second

control signal" limitations, in the claimed voltage regulators, the output voltage in the second state is maintained "substantially" at the regulated voltage rather than at the regulated voltage because an offset voltage (V_{OS}) is used to separate the first state of circuit operation from the second state. If there were no difference, the third circuit would always override the second circuit, and the voltage regulator would never operate in the first state as required by the claims. Indeed, the specification does not disclose how to construct a circuit that would operate at the same voltage in both states. *In re Certain Voltage Regulators*, 337-TA-564, Initial Determination (J.A. Tab Q), at 19-23. As Judge Harris explained:



Id. at 23 (emphasis added).

E. "first means" / "second means" / "third means"

Claim term	MPS Construction	Linear Construction
a first means for generating a voltage feedback signal indicative of the voltage at the output	This is a means-plus-function element governed by § 112, ¶ 6. The structures disclosed in the specification that correspond to the recited function are the following and their equivalents: (i) the combination of resistors 36A and 36B; (ii) the combination of resistors R1 and R2 and operational amplifier 602; and (iii) voltage feedback circuit 220.	This is a means-plus-function limitation, and it is to be construed to cover the corresponding structure(s) and equivalents thereof. The corresponding structures described in the specification include a resistor divider, with or without an operational amplifier, or other conventional voltage feedback circuits.
a second means for generating a first control signal … to maintain the	This is a means plus function element governed by § 112, ¶ 6. The structures in the specification that correspond to the recited	This is a means-plus-function limitation, and it is to be construed to cover the corresponding structure(s) and equivalents thereof.

Claim term	MPS Construction	Linear Construction
output terminal at the regulated voltage	function are the following and their equivalents: (i) the combination of drive circuit 20, transconductance amplifier 38, offset voltage V_{OS} 76, reference circuit 37, current source I1 72, current comparator 39, and constant off-time one shot circuit 25, which outputs the first control signal; (ii) combinations having a pulse-width modulator circuit that provides a pulse width modulated signal in response to a control signal, Patent col. 9:18-21; (iii) circuit 240 in Fig. 5.; (iv) the combination illustrated in Fig. 7 (resistors Rsense and R3, one-shot circuit 245, off time controller 250 and capacitor C_{CON}); (v) an "operational amplifier," Patent col. 10:15-16; and (vi) the circuitry described at col. 13, lines 36-46.	The corresponding structures described in the specification include: • As illustrated in Fig. 2, the combination of drive circuit 20, transconductance amplifier 38, offset voltage V_{os} 76, reference voltage 37, current comparator 39, a feedback current path I_{FB} between inductor L_1 32 and current comparator 39, and constant off-time one-shot circuit 25, which outputs the first control signal; • combinations having a pulse-width-modulator circuit or a variable-off-time one-shot circuit (*e.g.*, circuit 240 of Fig. 5 or the circuit described at 10:15-16); or • As illustrated in Fig. 7, the combination of resistors R_{SENSE} and R_3, V_{REF}, V_{OS}, current comparator 39, one-shot circuit 245, off-time controller 250, and capacitor C_{CON}.

Claim term	MPS Construction	Linear Construction
a third means for generating a second control signal ... the period of time having a duration which is a function of the current supplied to the load by the regulator	This is a means plus function element governed by § 112, ¶ 6. The structures in the specification that correspond to the recited functions are the following and their equivalents: (i) the combination of hysteretic comparator 74, the offset voltage 76, constant current source I_1 (72), logic gates 66, 68, and 69, and reference voltage 37, all as disclosed in Figure 2; and (ii) the circuitry disclosed in Figure 7 (72, 74, V_{OS}, 315, 316 and related sleep control logic).	This is a means-plus-function limitation, and it is to be construed to cover the corresponding structure(s) and equivalents thereof. The corresponding structures described in the specification include: • As illustrated in Fig. 2, hysteretic comparator 74, V_{REF}, current source I_1 72, and logic circuits 66, 68, and 69; • As illustrated in Fig. 7, combinations such as the circuitry including 72, 74, 315, 316, V_{REF}, and related sleep control logic; or • combinations such as those disclosed at 16:5-12.

The parties agree that the first, second, and third means are means-plus-function limitations, and are limited to the corresponding structure disclosed in the specification, and equivalents thereof. MPS proposes that the Court adopt the construction of these three terms previously given by the court in the *Impala* Litigation June 9, 1999, Claim Construction Order (J.A. Tab N). This should be non-controversial, as the *Impala* court adopted the constructions Linear had proposed for these terms and, not surprisingly, Linear never appealed those constructions. *See generally Linear Tech. Corp. v. Impala Linear,* 379 F.3d 1311 (Fed. Cir. 2004). Moreover, Linear has consistently represented in other litigations that the *Impala* court's constructions are correct. *See, e.g., In re Certain Voltage Regulators*, 337-TA-564, Initial Determination (J.A. Tab Q), at 11:

[redacted]

[redacted]

Despite its steadfast adherence to the *Impala* court's construction, Linear now wants a new construction of these terms.

The *Impala* court's identifications of structure are consistent with the other constructions MPS proposes. For example, the *Impala* court's construction of the third means includes the offset voltage V_{OS} 76. Linear now seeks to remove this structure from the *Impala* court's construction. But, as the '178 patent explains, "[o]ffset V_{OS} 76, which preferably is built into amplifier 38, level-shifts feedback voltage V_{FB} slightly below reference voltage V_{REF}, thus keeping the output of hysteretic comparator 74 high during high current conditions." '178 patent (J.A. Tab A), at 6:21-25. Thus, the offset voltage, along with other circuit components, is described by the specification as necessary to ensure that the claimed second state (*i.e.*, "sleep mode") is not entered during high load current conditions and that a different average voltage ("substantially" at the regulated voltage, but shifted by an amount determined by V_{OS}) is maintained during the second state. *See, e.g.*, '178 patent (J.A. Tab A), at 6:61-64, 7:22-26; *see also In re Certain Voltage Regulators*, 337-TA-564, Initial Determination (J.A. Tab Q), at 23:

[redacted]

Accordingly, MPS's proposed construction of third means includes the offset voltage as part of the corresponding means for the claimed function in accordance with the *Impala* court's Claim Construction Order. Linear's departure from the *Impala* court's construction is contradicted by the patent specification.

Because the specification supports the *Impala* court's construction, and Linear has consistently championed this construction in the past, the Court should decline to re-open this well-settled claim construction issue. In accordance with the *Impala* court's construction of these terms, the intrinsic support for the "first means" can be found, for example, at '178 patent

(J.A. Tab A), at 4:19-50, 6:17-25. The intrinsic support for the "second means" can be found, for example, at '178 patent (J.A. Tab A), at 4:19-67, 6:17-33, and the intrinsic support for the "third means" can be found, for example, at '178 patent (J.A. Tab A), at 6:34-7:37.

F. "switching voltage regulator"

MPS Construction	Linear Construction
a device or circuit that is capable of receiving a poorly specified and fluctuating input voltage and that provides a predetermined and essentially constant output voltage by controlling the opening and closing of a switch	A device or circuit that receives an input voltage and provides a predetermined and regulated output voltage by controlling the opening and closing of one or more switching transistors. (Predetermined means determined by design, and includes voltages that may be fixed or variable).

The '178 patent specification states that "[t]he purpose of a voltage regulator is to provide a predetermined and constant output voltage to a load from a poorly-specified and fluctuating input voltage source." '178 patent (J.A. Tab A), at 1:12-14. The specification further states that "the switching regulator employs a switch (*e.g.*, a power transistor) coupled either in series or parallel with the load. The regulator controls the turning ON and turning OFF of the switch in order to regulate the flow of power to the load." *Id.* at 1:20-24. Thus, the specification establishes that a "switching voltage regulator" is a device that is capable of receiving "a poorly specified and fluctuating input voltage" and "provid[ing] a predetermined and constant output voltage to a load" by "control[ling] the turning ON and turning OFF" of a switch. This is how MPS requests that the Court construe the term.

Linear, however, seeks to add language to indicate that the output voltage may be "fixed ***or variable***." This inconsistent language is at odds with a plain reading of the claims and the goal of the alleged invention. The output voltage cannot merely be "determined by design," but rather, must be predetermined and essentially constant. To permit the output voltage to vary without limit, as Linear would have it, would defeat the very purpose of a voltage regulator, which is to regulate the output voltage to a predetermined and essentially constant value.

G. "a pair of synchronously switched switching transistors"

MPS Construction	Linear Construction
a pair of switching transistors are "synchronously switched" when they are "driven out of phase to supply current at a regulated voltage to a load." "driven out of phase" means that the two switching transistors do not turn "on" and "off" at the same time at all times.	two switching transistors are synchronously switched when they are driven out of phase (i.e., one is ON and the other is OFF, except for deadtime) to supply current at a regulated voltage to a load

1. Overview

As previously noted, the preambles of the asserted claims of the Linear patents contain the language "including a pair of synchronously switched switching transistors." *See, e.g.*, '178 patent (J.A. Tab A), claim 1. Linear has proposed a construction for "synchronously switched" that would read in non-existent limitations, apparently in an attempt to distinguish the prior art. In particular, Linear seeks to import the limitations that (1) the switching transistors must operate exactly 180 degrees out of phase, (2) there can never be any time in which both switching transistors are turned "on," and (3) the switching transistors cannot be turned off simultaneously for any period longer than "dead time."

2. The Specification Defines "Synchronously-Switched Switch"; Dictionary Definitions Confirm The Transistors Do Not Need To Be 180 Degrees Out Of Phase

The Linear Patents define the term "synchronously switched," in the context of a "synchronously-switched switch," stating that "[a]s used herein, the term 'synchronously-switched switch' refers to a switch including two switching transistors that are driven out of phase to supply current at a regulated voltage to a load." '178 patent (J.A. Tab A) 7:40-43. "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Phillips,* 415 F.3d at 1316.

As evidenced by dictionary definitions, the ordinary meaning of "driven out of phase" to a person of skill in the art is not restricted to any specific phase (*e.g.*, 180 degrees as proposed by Linear), but encompasses any number of different phase values. For example, Wiley Electrical and Electronics Engineering Dictionary (2004) (J.A. Tab U) defines "phase" as:

> For a given periodic phenomenon . . . the portion of a complete cycle that has been completed, as measured from a given reference point. Two or more periodic quantities having the same frequency and waveshape that pass through corresponding values, such as maximas and minimas, at the same instant at all times are ***in-phase***. While periodic quantities that do not pass through corresponding values at the same instant at all times are ***out-of-phase***. A phase angle expresses the difference between the phases of two such quantities. Phase is usually expressed in degrees or radians, where a complete cycle is 360° or 2 Π, respectively.

(Emphasis added.)

3. Linear's Proposed Construction Would Result In The Preferred Embodiments Falling Outside The Patent Claims When They Entered What Linear Describes As "Sleep Mode"

As noted above, the preambles to the asserted claims contain the language "including a pair of synchronously switched switching transistors." *See*, *e.g.*, '178 patent (J.A. Tab A), claim 1. Linear claims as its invention a mode of operation ("sleep mode") where both switching transistors are turned "off." For example, the "third circuit" of claim 1 generates a "second control signal during a second state of circuit operation to cause both switching transistors to be simultaneously OFF for a period of time."

Under Linear's proposed construction, when the two switching transistors are simultaneously "off" during the claimed "sleep mode," they are not "driven out of phase" because they are not exactly 180 degrees apart in phase. Thus, according to Linear's construction, the switching transistors would not be "synchronously switched," and the regulator would not have a "switch circuit . . . including a pair of synchronously switched switching transistors," as required by the claim language. In other words, under Linear's proposed construction, at the point that a regulator entered what Linear describes as "sleep mode," the regulator would not fall within the scope of the patent claims. Since Linear's proposed

construction would exclude all preferred embodiments, it clearly is wrong. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (explaining that a construction that excludes the preferred embodiment "is rarely, if ever, correct and would require highly persuasive evidentiary support . . . ."). Alternatively, adopting Linear's construction necessarily would establish that the accused MP1543 part cannot infringe any asserted claim.

4. Linear's Attempt To Import A "Dead Time" Limitation Into The Definition Of "Synchronously Switched" Is Without Merit

There is no basis for Linear's attempt to interject the notion of "dead time" into the construction of the term "synchronously switched." There is nothing in the term "driven out of phase" that excludes "dead time." Linear has not offered any dictionary definition for "driven out of phase," much less one that suggests the concept of "dead time" is connected in any way to the concept of transistors being "driven out of phase."

5. Conclusion

MPS's proposed construction for "synchronously switched" comports with patent specification's definition of the term "synchronously-switched switch" and the ordinary meaning of the term "driven out of phase." Linear's proposed construction does not.

H. "coupled"

MPS Construction	Linear Construction
circuit elements are "coupled" when they are so arranged that energy can transfer electrically or magnetically from one to another	circuit elements are coupled when a current path exists between them

The preambles of the asserted claims include the language "a switch circuit coupled to receive an input voltage and including a pair of synchronously switched switching transistors." *See, e.g.*, '178 patent (J.A. Tab A), claim 1. The term "coupled" has a plain and ordinary meaning to electrical engineers – circuits elements are coupled when energy can transfer from one to the other, as discussed below. This coupling can be electrical (*e.g.*, by a direct wired connection) or magnetic/inductive (*e.g.*, through a transformer).

In an effort to avoid a prior art reference, Linear proposes a construction that would artificially and improperly narrow the term "coupled" in the Linear Patents so as to limit it to electrical coupling and exclude magnetic or inductive coupling. However, "the [Federal Circuit] has admonished against judicial rewriting of claims to preserve validity. Accordingly, unless the court concludes, after applying all the available tools of claim construction, that the claim is still ambiguous, the axiom regarding the construction to preserve the validity of the claim does not apply." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 911 (Fed. Cir. 2004).

The term "coupled" is commonly understood as including both electrical and magnetic/inductive coupling. This is consistent with the definitions for the term that appear in numerous technical dictionaries. *See, e.g.,* Gibilisco, Illustrated Dictionary of Electronics, 8th ed. (2001) (J.A. Tab S) (emphasis added) ("***coupled circuits***: circuits between which energy is transferred electrostatically, ***electromagnetically***, by some combination of the two, or by direct connection"); McGraw-Hill Dictionary of Electronics and Computer Technology (1984) (J.A. Tab T) (emphasis added) (***"coupled circuits***: two or more electric circuits so arranged that energy can transfer electrically or ***magnetically*** from one to another; ***inductive coupling***: coupling of two circuits by means of the mutual ***inductance provided by a transformer***. Also known as transformer coupling"); Wiley Electrical and Electronics Engineering Dictionary (2004) (J.A. Tab U) (emphasis added) ("***couple***: 2. That which has been joined, linked, or connected in a manner which allows the transfer of energy. For example, coupled circuits; ***coupled circuits***: Two or more electric circuits which are coupled. Such coupling may be capacitive, ***inductive***, conductive, and so on").

Indeed, the Federal Circuit has previously construed "coupled" nearly identically in another case. *See Tegal Corp. v. Tokyo Electron America, Inc.*, 257 F.3d 1331, 1341, 1434 n.6 (Fed. Cir. 2001) (construing "coupled" to mean "electrically connected or connected by a conductive path, capacitively, ***inductively***, or by any other means of transferring energy") (emphasis added).

"When a claim term has an accepted scientific meaning, that meaning is generally not subject to restriction to the specific examples in the specification." *Glaxo Wellcome Inc. v. Andrx Pharms., Inc.*, 344 F.3d 1226, 1233 (Fed. Cir. 2003). The ordinary meaning of "coupled" includes circuits that are either electrically coupled or magnetic coupled. Linear's proposed construction is nothing more than an attempt to import the preferred embodiment into the claims.

The Federal Circuit has explained that "the line between construing terms and importing limitations can be discerned with reasonable certainty and predictability if the ***court's focus remains on understanding how a person of ordinary skill in the art would understand the claim terms***." *Phillips,* 415 F.3d at 1323 (emphasis added). Here, the ordinary meaning of the term "coupled" is clear. There is nothing in the specification or the prosecution history that suggests, much less convincingly establishes, that Linear intended to be its "own lexicographer" and provide a special definition for the common term "coupled." Thus, longstanding claim construction rules dictate that Linear's improper attempt to narrow the scope of the term "coupled" be denied.

I. "load" / "output terminal"

Claim Term	MPS Construction	Linear Construction
load	a device, circuit or system that consumes electric power; not part of the regulator structure	a device, circuit or system coupled to the output terminal to which the regulator can supply current
output terminal	a specific point of the switching voltage regulator that is directly connected to the load	a point or node of the switching regulator to which the load is coupled

"The purpose of a voltage regulator is to provide a predetermined and constant output voltage to a load." '178 patent (J.A. Tab A), at 1:12-13. Thus, the term "load" is used in the Linear Patents in its ordinary fashion, to refer to a device, circuit or system that consumes electric power; not part of the regulator structure. *See, e.g.,* the McGraw-Hill Dictionary of Electronics and Computer Terminology (1984) (J.A. Tab T), which defines ***load*** to mean "a

device that consumes electric power." Likewise, Wiley Electrical and Electronics Engineering Dictionary (2004) (J.A. Tab U) defines ***load*** as "2. [a]ny component, circuit, device . . . which consumes . . . or otherwise utilizes power, especially electricity." This is consistent with the Federal Circuit's *Impala* opinion, which states that "voltage regulators . . . are designed to provide a predetermined and constant voltage output from a fluctuating input voltage source, such as a battery, to ***an energy consuming device, called a 'load.'***" 379 F.3d at 1316 (emphasis added).

Linear's proposed construction for "load" is vague and essentially meaningless, because it suggests that virtually anything can be a "load." Furthermore, given the broad definition of "coupled" (even as Linear would have it construed – "circuit elements are coupled when a current path exists between them"), Linear's construction would result in there being multiple "loads." For example, a current path exists between the regulator's output terminal and the internal circuitry of the voltage regulator. Thus, even according to Linear's improperly narrow definition of "coupled," the internal circuitry could be a "load." Similarly, a current path exists between the input voltage source, *e.g.*, a battery, and the output terminal. Thus, even the input battery could be a "load" according to Linear, which is nonsensical.

For similar reasons, Linear's proposed construction of "output terminal" – "a point or node of the switching regulator to which the load is coupled" – is incorrect. Since a substantial portion of the internal circuitry of the voltage regulator is "coupled" to the load, Linear's construction would mean that, for example, that the junction between R_1 and R_2 in Figure 2 of the Linear Patents, the negative input of hysteretic comparator 74, and the common connection between the two switching transistors are all appropriately identified as "output terminals." Those are absurd consequences of a faulty construction.

V. CONCLUSION

For the reasons set forth above, MPS respectfully submits that the Court adopt its proposed constructions for the identified claim terms.

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IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

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EXHIBIT A

Service: **Get by LEXSEE®**
Citation: **2004 U.S. District LEXIS 23230**

*2004 U.S. Dist. LEXIS 23230, **

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH, Plaintiffs, v. RAMBUS INC., Defendant.

View the Full Docket from LexisNexis CourtLink for 5:00cv20905
No. CV-00-20905 RMW

UNITED STATES DISTRICT COURT FOR THE NORTHERN DISTRICT OF CALIFORNIA, SAN JOSE DIVISION

2004 U.S. Dist. LEXIS 23230

November 15, 2004, Decided

SUBSEQUENT HISTORY: Related proceeding at Samsung Elecs. Co. v. Rambus Inc., 386 F. Supp. 2d 708, 2005 U.S. Dist. LEXIS 20337 (E.D. Va., 2005)
Findings of fact/conclusions of law at Hynix Semiconductor, Inc. v. Rambus Inc., 2006 U.S. Dist. LEXIS 30690 (N.D. Cal., Jan. 4, 2006)
Related proceeding at Micron Tech., Inc. v. Rambus Inc., 409 F. Supp. 2d 552, 2006 U.S. Dist. LEXIS 962 (D. Del., 2006)

DISPOSITION: Court interpreted disputed claim terms.

CASE SUMMARY

PROCEDURAL POSTURE: At issue was the construction of disputed terms used in 15 patents descending from a single patent application, U.S. Patent Appl. No. 07/510,898 ('898 application). Defendant assignee of the '898 application and plaintiffs briefed the issues and presented evidence at a claim construction hearing and upon consideration of the arguments of counsel, and the disputed terms in the patent claims were construed.

OVERVIEW: Defendant requested, inter alia, that the district court adopt the Federal Circuit's construction of "integrated circuit device," to have its ordinary meaning to one of skill in the art--"a circuit constructed on a single monolithic substrate, commonly called a chip." In turn the plaintiffs proposed that "integrated circuit device" be construed as "a device that includes one or more integrated circuits." The district court held that even assuming that the Federal Circuit's construction was dicta, the Federal Circuit's reasoning remained applicable, namely that there was no justification for reading unstated limitations into claim and concluded that this reasoning was persuasive. Likewise, the court determined that "operation code" carried its ordinary meaning, as the claim language, the specification, and the prosecution history did not suggest that the patent used "operation code" in a manner inconsistent with its ordinary meaning. Therefore, the court found "operation code" was properly construed as "one or more bits to specify a type of action."

OUTCOME: The district court issued its construction of disputed terms including, "integrated circuit device" and "operation code."

CORE TERMS: bus, memory, clock, access time, specification, external, signal, register,

patent, synchronous, packet, invention, block, precharge, output, multiplexed, embodiment, timing, integrated, bit, proposed construction, multiplexing, transferred, cycle, specify, chip, slave, stored, transpire, input

LexisNexis(R) Headnotes ♦ Hide Headnotes

Patent Law > Claims & Specifications > Enablement Requirement > General Overview

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN1 The construction of patent claim terms is a matter of law for the court. As the language of the claim defines the scope of the claim, claim construction analysis begins with the words of the claim. As a general rule, claim language carries the meaning of the words in their normal usage in the field of the invention. However, where the intrinsic evidence shows that the specification uses the words in a manner clearly inconsistent with their ordinary meaning, the ordinary meaning must be rejected. More Like This Headnote

Patent Law > Claims & Specifications > Description Requirement > General Overview

Patent Law > Inequitable Conduct > General Overview

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN2 Inventors may act as their own lexicographers and use the specification to supply implicitly or explicitly new meanings for claim terms. Nevertheless, where a patentee has elected to be a lexicographer by providing a definition in the specification for a claim term, the patentee's lexicography must appear with reasonable clarity, deliberateness, and precision. If the patentee provides such a clear definition, reference to the written description is required, because only there is the claim term defined as it is used by the patentee. More Like This Headnote

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN3 Claim construction is guided by two fundamental, sometimes conflicting, canons: (a) one may not read a limitation into a claim from the written description, but (b) one may look to the written description to define a term already in a claim limitation, for a claim must be read in view of the specification of which it is a part. Notably, it is manifest that a claim must explicitly recite a term in need of definition before a definition may enter the claim from the written description. The intrinsic evidence, and, in some cases, the extrinsic evidence, can shed light on the meaning of the terms recited in a claim, either by confirming the ordinary meaning of the claim terms or by providing special meaning for claim terms. More Like This Headnote

Governments > Courts > Judicial Precedents

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN4 Consulting the written description and prosecution history prior to ascertaining the ordinary meaning invites a violation of our precedent counseling against importing limitations into the claims. Rather, the full breadth of the limitations intended by the inventor will be more accurately guided by examining relevant dictionaries, encyclopedias and treatises publicly available at the time the patent is issued. Such references are unbiased reflections of common understanding not influenced by expert testimony or events subsequent to the fixing of the intrinsic record by the grant of the patent, not colored by the motives of the parties, and not inspired by litigation. Examining these references together with the intrinsic evidence allows a court to construe terms more consistently with the inventor's use of the terms, more accurately determine the full breadth of the limitations, and avoid the improper importation of unintended limitations from the written description into the claims. More Like This Headnote

Governments > Courts > Judicial Precedents

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN5 Where the United States Court of Appeals for the Federal Circuit has already construed certain claim terms, these constructions are done as a matter of law and are given stare decisis effect. More Like This Headnote

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN6 Unless compelled otherwise, a court will give a claim term the full range of its ordinary meaning as understood by persons skilled in the relevant art. More Like This Headnote

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN7 When a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term by implication. More Like This Headnote

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN8 A limitation upon a claim term may be implied from its existence in the sole preferred embodiment when no other broader concept was described as embodying the applicant's invention, or shown in any of the drawings, or presented for examination. More Like This Headnote

Patent Law > Infringement Actions > Claim Interpretation > General Overview

HN9 The law does not require an applicant describe in the specification every conceivable and possible future embodiment of his invention. More Like This Headnote

Patent Law > Claims & Specifications > Description Requirement > General Overview

Patent Law > Infringement Actions > Claim Interpretation > General Overview

Patent Law > U.S. Patent & Trademark Office Proceedings > Reissues > General Overview

HN10 Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question. More Like This Headnote

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JUDGES: RONALD M. WHYTE, United States District Judge.

OPINION BY: RONALD M. WHYTE

OPINION: CLAIM CONSTRUCTION ORDER

At issue is the construction of disputed terms used in 15 patents descending from a single patent application, **[*5]** U.S. Patent Appl. No. 07/510,898 ("the '898 application"). Defendant Rambus Inc. and plaintiffs Hynix Semiconductor Inc., Hynix Semiconductor America Inc., Hynix Semiconductor U.K. Ltd., and Hynix Semiconductor Deutschland Gmbh ("Hynix") briefed the issues and presented evidence at a claim construction hearing on March 23, 2004. The court has read the moving and responding papers, including the patents-in-suit and the relevant prosecution history, considered the arguments of counsel, and now construes the disputed terms in the claims.

I. BACKGROUND

A. Factual background

Rambus is the assignee of several patents covering Synchronous Dynamic Random Access Memory ("SDRAM") chips and related interface and memory control technology. Second Am. Compl. P 10. In the vast majority of computers, Dynamic Random Access Memory ("DRAM") serves as the main memory for temporary storage of data currently being utilized by the Central Processing Unit ("CPU" or "processor"). In contrast to a hard drive, which permits long-term "non-volatile" storage, DRAMs do not retain information written to them once the computer is turned off. n1 Information on a hard drive, however, must be transferred **[*6]** to a main memory composed of DRAM before it can be accessed by the CPU. Thus, in most computers, a main memory composed of DRAM is the principal storage location for computer programs that are running at a given time, along with the data on which the programs operate.

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n1 DRAMs lose their contents once power is no longer applied to the circuit because each bit is stored as a charge in a memory cell composed of a transistor and a capacitor. While a system is running the charge that creates each bit deteriorates. As a result, all DRAM memory locations must periodically have their charges refreshed.

- - - - - - - - - - - - - - End Footnotes- - - - - - - - - - - - - - -

DRAMs are generally arranged in two-dimensional arrays of memory cells designated by rows and columns. Exactly one bit of information is stored at each row-column intersection. An individual datum stored in the array is accessed by supplying the DRAM with the row and

column address corresponding to the location of the memory cell to be accessed. Control information instructs the DRAM on what operation is to be performed. **[*7]** Basic operations include read accesses, where data is retrieved from the DRAM cells, and write operations, where data is written to selected cells.

The patented inventions deal with computer memory devices called Synchronous DRAM ("SDRAM"). SDRAM is a type of memory designed to improve the speed and efficiency of data transfers to and from devices that access the memory. In most operational circumstances, when appropriately designed for use in a general purpose computer, SDRAM devices provide a performance advantage over earlier DRAM devices. The initial Rambus application was the '898 application filed on April 18, 1990. Rambus asserts that the SDRAM patents are entitled to that date as their effective filing date. Rambus claims patents for "the interface circuitry that connects DRAMs to the CPUs with which they communicate and that connects them to the overall systems in which they reside." Def.'s Opening Claim Const. Br. ("CC Brief") at 3. Rambus claims eleven distinct groups of inventions stemming from the '898 application. Each of these claimed inventions addresses a "memory bottleneck" problem, where a busmaster n2 normally has to wait for data to be available for transfer to **[*8]** or from the DRAM. n3 Specifically, Rambus contends that by using its invention, DRAMs are able to provide data to a busmaster as fast as that processor can process it, thus keeping pace with the ever-increasing speed of CPUs. Each patent in suit describes the same field of invention:

> An integrated circuit bus interface for computer and video systems . . . which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability. A new method of physically implementing the bus architecture is also described.

U.S. Patent No. 5,953,263 ("the '263 patent"), col. 1, 11. 9-15. n4

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n2 Initiators of data transfers are called busmasters.

n3 Rambus asserts that using all eleven inventions results in the most effective speed and efficiency but that each invention may be used individually or in combination. CC Br. at 5.

n4 Hynix references to the Rambus patent specification are to U.S. Patent No. 6,101,152 ("the '152 patent"); Rambus references the '263 patent. For ease of citation, all references to the specification will be to the '263 patent.

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In the 1990's, the Joint Electronic Devices Engineering Council ("JEDEC") coordinated the development of technology standards for SDRAM chips. Second Am. Compl. P 12. Plaintiff alleges, *inter alia*, that as a member of JEDEC, Rambus used information gained from the standards-setting process to secretly and fraudulently secure the patents at issue ("SDRAM

patents"), and, therefore, market power. Plaintiff further alleges that these actions were taken in violation of JEDEC's rules and various federal and state laws. Second Am. Compl. PP 11-13. n5

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n5 Plaintiff also apparently alleges that Rambus disparaged technology standards for chips that would not be covered by Rambus's patents.

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B. Legal background

Certain terms in the same family of disputed patents have already been construed by the Eastern District of Virginia in Rambus, Inc. v. Infineon Techs. AG, 2001 U.S. Dist. LEXIS 10990, 2001 WL 34138091 (E.D. Va. 2001) ("*Infineon I*"). Specifically, the terms "bus," "block size information," "read request," "write **[*10]** request," "transaction request," "first external clock signal," "second external clock signal" and "integrated circuit device" were construed in *Infineon I*. The district court in *Infineon I* granted summary judgment of non-infringement for Infineon, entered judgment on a jury verdict of fraud under Virginia state law for conduct occurring during JEDEC SDRAM standardization proceedings, and granted judgment as a matter of law in favor of Rambus, overturning a jury verdict of fraud committed during consideration of DDR-SDRAM standards. n6 Rambus, *inter alia*, appealed the district court's claim construction of the terms "integrated circuit device," "read request," "write request," "transaction request," and "bus." *See* Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081, 1088 (Fed. Cir. 2003) ("*Infineon II*"). The Federal Circuit reversed the district court and disagreed with the district court's construction of each of these terms, vacated the judgment of noninfringement, vacated the jury's SDRAM fraud verdict, and remanded for further proceedings under the revised claim construction. *See id.* at 1106. Of these terms, the parties dispute only **[*11]** the proper construction of "integrated circuit device."

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n6 The district court found that substantial evidence did not support the jury's verdict because Rambus left JEDEC before work officially began on the DDR-SDRAM standard. *See* Rambus, Inc. v. Infineon Techs. AG, 164 F. Supp. 2d 743, 767 (E.D. Va. 2001).

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On November 21, 2001 this court granted plaintiff's motion for partial summary judgment of non-infringement with respect to twenty-seven claims from the patents-in-suit. In its November 2001 order, the court concluded that the doctrine of collateral estoppel barred Rambus from re-litigating claim construction and infringement of certain representative claims of the patents-in-suit. The court's earlier order was based on the claim construction and judgment of non-infringement entered against Rambus in *Infineon I*. In light of the Federal Circuit's January 29, 2003 order reversing *Infineon I*'s construction of certain terms in the asserted claims, the court on July 25, 2003 vacated in **[*12]** its entirety the November 21, 2001 order.

II. ANALYSIS

HN1 The construction of patent claim terms is a matter of law for the court. Markman v.

Westview Instruments, Inc., 517 U.S. 370, 372, 134 L. Ed. 2d 577, 116 S. Ct. 1384 (1996) ("*Markman II*"). As the language of the claim defines the scope of the claim, claim construction analysis begins with the words of the claim. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002); *ASM Am., Inc. v. Genus, Inc.*, 260 F. Supp. 2d 827, 831 (N.D. Cal. 2002). "As a general rule, claim language carries the meaning of the words in their normal usage in the field of the invention." *Infineon II*, 318 F.3d at 1088 (citing *Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1299 (Fed. Cir. 1999)). In other words, claim language is construed to mean "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." *Id.* (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 986 (Fed. Cir. 1995) ("*Markman I*")).

However, where the intrinsic evidence shows that the specification uses the words in a manner **[*13]** clearly inconsistent with their ordinary meaning, the ordinary meaning must be rejected. *See Tex. Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1204 (Fed. Cir. 2002). In short, HN2 "inventors may act as their own lexicographers and use the specification to supply implicitly or explicitly new meanings for claim terms." *Infineon II*, 318 F.3d at 1088. Nevertheless, where a patentee has elected to be a lexicographer by providing a definition in the specification for a claim term, the patentee's lexicography must appear "with reasonable clarity, deliberateness, and precision." *Renishaw PLC v. Marposs Societa' Per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998) (quoting *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994)). If the patentee provides such a clear definition, reference to the written description is required, "because only there is the claim term defined as it is used by the patentee." *Id.* Thus, HN3 claim construction is guided by two fundamental, sometimes conflicting, canons: "(a) one may not read a limitation into a claim from the written description, but (b) one may look to the written description to define **[*14]** a term already in a claim limitation, for a claim must be read in view of the specification of which it is a part." *Renishaw*, 158 F.3d at 1248 (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Markman I*, 52 F.3d at 979-80.

Notably, "it is manifest that a claim must explicitly recite a term in need of definition before a definition may enter the claim from the written description." *Renishaw*, 158 F.3d at 1248. "The intrinsic evidence, and, in some cases, the extrinsic evidence, can shed light on the meaning of the terms recited in a claim, either by confirming the ordinary meaning of the claim terms or by providing special meaning for claim terms." *Id.* (citing *Vitronics*, 90 F.3d at 1583).

HN4 Consulting the written description and prosecution history prior to ascertaining the ordinary meaning "invites a violation of our precedent counseling against importing limitations into the claims." *Texas Digital*, 308 F.3d at 1204 (citations omitted). Rather, the full breadth of the limitations intended by the inventor will be more accurately guided by examining **[*15]** relevant dictionaries, encyclopedias and treatises "publicly available at the time the patent is issued. . . ." *Id.* at 1203. "Such references are unbiased reflections of common understanding not influenced by expert testimony or events subsequent to the fixing of the intrinsic record by the grant of the patent, not colored by the motives [of] the parties, and not inspired by litigation." *Id.* Examining these references together with the intrinsic evidence allows a court to construe terms more consistently with the inventor's use of the terms, more accurately determine the full breadth of the limitations, and avoid the improper importation of unintended limitations from the written description into the claims. *Id.* at 1205.

HN5 Since the Federal Circuit has already construed certain claim terms, these constructions are done as a matter of law and are given *stare decisis* effect. *See Markman II*, 517 U.S. at 390; *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1455 (Fed. Cir. 1998) (noting that in *Markman II* "the Supreme Court endorsed this court's role in providing national uniformity to the construction of a **[*16]** patent claim."); *Key Pharms. v. Hercon Lab. Corp.*, 161 F.3d

709, 716 (Fed. Cir. 1998).

1. Device

a. Proposed constructions

Hynix asserts that "device" should be construed as "electronic circuits or components physically connected in a unit, with an interface to a bus having a multiplexed set of signal lines used to transmit substantially all address, data, and control information, and containing substantially fewer lines than the number of bits in a single address." Hynix contends that the definition of "device" is a common denominator in several terms, and, therefore, should be separately defined and incorporated into each of the asserted claims.

Rambus counters that "device," by itself, is not a proper term for construction. Specifically, it contends that although the word "device" does appear in the claims, it only appears in conjunction with other terms, *i.e.* "integrated circuit device," "memory device," and "synchronous memory device." Rambus argues that it would be improper for the term "device" to be construed separately from the context in which it appears in the claims. Thus, Rambus argues that only "integrated circuit device," "memory **[*17]** device" and "synchronous memory device" should be construed. Rambus also submits that Hynix's proffered construction of "device" would read multiplexing into the claims, and that such a construction would be at odds with the Federal Circuit's decision.

b. Federal Circuit

The Federal Circuit reversed *Infineon I*'s construction of "bus" to mean "a multiplexed set of signal lines used to transmit address, data and control information." *Infineon II*, 318 F.3d at 1094. n7 The district court held that the patentees acted as their own lexicographer by redefining "bus" to mean a "multiplexed bus." When the Federal Circuit overturned this construction, it noted that "the claims do not specify that the bus multiplexes address, data and control information. *See* '918 patent, col. 26, 11. 19-27. Nothing in the claims compels a definition different from the ordinary meaning of "bus.'" *Id.*

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n7 In the context of this patent family "multiplexing refers to the sharing of a single set of lines to send multiple types of information." *Infineon II*, 318 F.3d at 1094. The multiple types of information under the district court's construction included address, data and control information.

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The Federal Circuit acknowledged that the Summary of the Invention and Detailed Description in the specification supported an inference that "bus" was limited to a multiplexing bus, but went on to note that "the remainder of the specification and prosecution history shows that Rambus did not clearly disclaim or disavow such claim scope in this case." *Infineon II*, 318 F.3d at 1094-95 (citing *Inverness Med. Switz. GmbH v. Princeton Biomeditech Corp.*, 309 F.3d 1365, 1372 (Fed. Cir. 2002) (statements made during prosecution not clear and unambiguous disclaimer of claim scope)). The Federal Circuit found that multiplexing was not a requirement in all of Rambus's claims. Specifically, at least two original claims of the '898 application recite a multiplexed bus, while others do not. n8 In addition, the court of appeals reasoned that Rambus distinguished certain claims as reciting a multiplexed bus because Rambus viewed "bus" as having its ordinary meaning. "Indeed, it is because Rambus viewed bus' under its ordinary meaning that Rambus specified -- in the

claim language -- that the inventive multiplexing bus carries substantially all address, data, and **[*19]** control information and that the bus operates without the need for device-select lines." *Id.* at 1095.

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n8 For example, original claim 1 of the '898 application recites a "bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said memory device." *Infineon II*, 318 F.3d at 1095. Other original claims require that the "bus carry . . . device-select information without the need for separate device-select lines connected directly to individual semiconductor devices." *Id.*

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The Federal Circuit also noted that, in prosecuting the claims of U.S. Patent No. 5,841,580 ("the '580 patent"), the parent of the '263 patent, "the PTO issued a two-way restriction, dividing the claims into two distinct groups: a multiplexing bus group (Group I) and a latency invention group (Group II)." *Id.* at 1095. "Rambus elected to prosecute the latency claims from Group II in the '580 patent. Therefore, the claims of the '580 patent do not **[*20]** require a multiplexing bus." *Id.* As the claims of the '580 patent recite a bus, the court of appeals concluded that the PTO understood that "bus" was not limited to a multiplexing bus. *Id.* "The specification and prosecution histories, taken in their entirety, convince this court that Rambus did not redefine bus' to be a multiplexing bus in the patents-in-suit." *Id.* "The term bus' carries its ordinary meaning as a set of signal lines to which a number of devices are connected, and over which information is transferred between devices." *Id.* at 1095.

Here, rather than applying a multiplexing limitation to the bus, Hynix asserts that multiplexing should limit the term "device." It remains unclear how "electronic circuits or components physically connected in a unit, with an interface to a bus having a multiplexed set of signal lines" is materially different from limiting the term "bus" to a "multiplexed bus." Although the focus is on the memory chip itself rather than its operational means of connection to the bus, the end result remains the same -- the bus upon which the devices reside in the patents at issue would necessarily be a multiplexed bus. This **[*21]** end result, a multiplexed bus as part of the claim limitations, was rejected by the Federal Circuit.

Hynix relies on the Summary of the Invention, the Detailed Description, and the recitation of the objects of the invention in support of its contention that Rambus has acted as its own lexicographer in defining "device." This is largely the same material in the specification that the Federal Circuit found inadequate to support the multiplexing limitation on the term "bus." *See Infineon II*, 318 F.3d at 1094-95. In addition, U.S. Patent No. 6,101,152 ("the '152 patent") descends from the same '580 patent that does not require a multiplexing bus. The court, therefore, does not read a multiplexed bus limitation into the term "device." "Device" must be construed in the context of "integrated circuit device," "memory device," or "synchronous memory device."

2. Integrated Circuit Device

a. Proposed constructions

Rambus requests that this court adopt the Federal Circuit's construction of "integrated circuit device," as "a circuit constructed on a single monolithic substrate, commonly called a chip.'" CC Br. at 14; *Infineon II*, 318 F.3d at 1091. **[*22]** Hynix proposes that "integrated circuit device" be construed as "a device that includes one or more integrated circuits."

b. Federal Circuit

The district court in *Infineon I* construed "integrated circuit device" in the related U.S. Patent No. 5,954,804 ("the '804 patent) as requiring "a device ID register, interface circuitry and comparison circuitry." 2001 U.S. Dist. LEXIS 10990, 2001 WL 34138091 at *28. Hynix contends that the Federal Circuit's construction of integrated circuit device was dictum not essential to its decision. Specifically, Hynix argues that here, limiting integrated circuit device as including an "identification register" is not at issue.

The Federal Circuit examined the language of claim 26 of the '804 patent n9 and found that the claim language did not support the district court's construction, noting that the terms "comparison circuitry" and "device identification register" do not appear anywhere in the text of the claim. *Infineon II*, 318 F.3d at 1089. The Federal Circuit also noted that there was "no justification for reading unstated limitations into claim 26," and construed "integrated circuit device" to have its ordinary meaning to one of skill **[*23]** in the art -- "a circuit constructed on a single monolithic substrate, commonly called a chip.'" *Id.* at 1090-91 (citing *Rambus, Inc. v. Infineon Techs. AG*, 2001 U.S. Dist. LEXIS 10990, *89, No. 3:00cv524 (E.D. Va. 2001)); *cf.* THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONIC TERMS 662 (5th ed. 1993); IBM DICTIONARY OF COMPUTING 347 (10th ed. 1994); *see also Tex. Digital*, 308 F.3d at 1202 HN6("unless compelled otherwise, a court will give a claim term the full range of its ordinary meaning as understood by persons skilled in the relevant art."). Even assuming that the Federal Circuit's construction is dicta, the Federal Circuit's reasoning remains applicable to the present matter, and the reasoning is persuasive. The court, as urged by Rambus, construes "integrated circuit device" as "a circuit constructed on a single monolithic substrate, commonly called a chip.'"

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n9 Claim 26 recites:

> 26. An *integrated circuit device* having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:
>
> a first internal register to store a value which is representative of a number of clock cycles to transpire before the integrated circuit device responds to a read request;
>
> delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals; and
>
> interface circuitry, coupled to the external bus to receive a read request, the interface circuitry includes a plurality of output drivers, coupled to the external bus, to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register. U.S. Patent No. 5,954,804 (issued Sept. 21, 1999) (emph. added).

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3. Synchronous Memory Device

a. Proposed constructions

Hynix argues that "synchronous memory device" should be construed to mean "a memory device in which an external clock is used for timing purposes." Rambus counters that the term should be construed as "a memory device in which address, input data and control signals are recognized and output data signals are transferred in response to an external clock." The parties agree that a "synchronous" memory device is one in which at least some operations are synchronous with respect to an external clock. *See, e.g.*, Hynix's Resp. CC Br. at 12. The parties disagree, however, over whether "synchronous" requires that all operations on the memory device be timed with respect to an external clock, or whether some operations on the memory device can be "asynchronous" while executing other operations as "synchronous.' n10

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n10 Both parties agree that "synchronized" means "having a known timing relationship with respect to." Opp. at 6 n.2.

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As noted during **[*25]** the tutorial, DRAM in the early 1990's were asynchronous, although not called such, until the advent of Synchronous DRAM. Thus, the development and meaning of "Synchronous DRAM" is a relatively recent phenomenon.

b. Claim language

11 of the 15 patents in suit have claims reciting the limitation "synchronous memory device." Claim 1 and asserted claim 2 of the '263 patent, for instance, recite:

> 1. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
>
> > a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.
>
> 2. The synchronous memory device of claim 1 further including output drivers, coupled to an external bus, to output data on the bus, in response to the read request, synchronously with respect to an external clock.

Although claiming a "synchronous memory device," nothing in the text of claim 1, upon which claim 2 depends, excludes some asynchronous operations. In addition, claim 1 does

not explicitly require that address, input data and control signals be provided synchronously. **[*26]** Notably, claim 1 uses the term "comprises" in describing a memory device with a programmable register, thus apparently not closing the claim to asynchronous elements. *See* *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1271 (Fed. Cir. 1986) ("The term comprising' denotes a patent claim as being open,' meaning that the recitation of structure in the claim is open to additional structural elements not explicitly mentioned."); M.P.E.P. § 2173.05(h) (6th Ed. 1996); *see also* '152 patent, cl. 11.

c. Ordinary meaning

Hynix offers definitions of "synchronous" from two dictionaries. Webster's Ninth New Collegiate Dictionary (2d ed. 1989) defines synchronous as:

> 1: happening, existing, or arising at precisely the same time; 2: recurring or operating at exactly the same periods; . . . 4a: having the same period; *also*: having the same period and phase.

The Oxford English Dictionary (2d ed. 1989) defines synchronous as:

> 1.a. Existing or happening at the same time; coincident in time; belonging to the same period, or occurring at the same moment, of time; contemporary; simultaneous . . .; b. . . . Relating to or treating of different **[*27]** events or things belonging to the same time or period; involving or indicating contemporaneous or simultaneous occurrence. . . .
>
> 2.a. Recurring at the same successive instants of time; keeping time *with*; going on at the same rate and exactly together; having coincident periods, as two sets of vibrations or the like. . . . b. *Electr*. Applied to alternating currents having coincident periods; also to a machine or motor working in time with the alternations of current. . . . c. *Computer* and *Telecommunications*. Of apparatus or methods of working: making use of equally spaced pulses that govern the timing of operations. . . .

The Authoritative Dictionary of IEEE (Institute of Electrical and Electronics Engineering) Standards Terms (5th ed. 1993) ("IEEE Dictionary") defines "synchronous" as:

> A mode of transmission in which the sending and receiving terminal equipment are operating continuously at the same rate and are maintained in a desired phase relationship by an appropriate means.

Rambus offers the IEEE Dictionary (4th ed. 1988) definition of "synchronous computer," a "computer in which each event or the performance of each operation, starts as a **[*28]** result of a signal generated by a clock." *See also* THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 1141 (7th ed. 2000).

In contrast, the IEEE Dictionary (5th ed. 1993) defines "synchronous device" more broadly, as "[a] device whose speed of operation is related to the rest of the system to which the device is connected." *See also* THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 1141 (7th ed. 2000).

Rambus argues that "synchronous memory device" should be defined in the same way as "synchronous computer." In addition, Rambus argues that articles cited by Hynix's expert, David Taylor, all refer to DRAMs that persons of ordinary skill in the art would refer to as "asynchronous DRAMs." Murphy Reply Decl. P 13. In contrast, the IEEE definition of "synchronous device" does not require that every operation be synchronous, but that the device's "speed of operation" be related to the rest of the system to which it is connected. Hynix also suggests that DRAMs in the late 1980's and early 1990's that timed all inputs and outputs to an external clock were more often referred to as "fully synchronous." n11 Taylor Decl. P 21.

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n11 The first patent issuing from the original '898 application, U.S. Pat. No. 5,319,755 ("the '755 patent"), issued on June 7, 1994.

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As discussed *supra*, the Federal Circuit construed "bus" as having its ordinary meaning, and not limited to a "multiplexed bus." Here, there is no clear statement that a "synchronous memory device" must exclude asynchronous functions. Considering the changing nature of bus architecture, the scope of claims in Rambus's related SDRAM patents covering both memory devices and synchronous memory devices, and the lack of any clear statement defining "synchronous memory device" as requiring that all operations be synchronous, a broader construction of memory device than the one offered by Rambus is warranted.

d. Specification

The specification does not use or define the term "synchronous memory device." Rather, Rambus contends that numerous references in the specification imply a memory device where address, input data and control signals are required to be synchronous. The specification references that Rambus cites, however, in large part discuss a clocking scheme in the context of a multiplexed bus architecture. *See, e.g.*, '263 patent col. 8, 11. 8-32. The specification states, for instance, that "another object of this invention is to provide a method for transferring address, **[*30]** data and control information over a relatively narrow bus and to provide a method of bus arbitration when multiple devices seek to use the bus simultaneously." *Id.* at col. 3, 11. 25-29. The implication that address, data and control information must be asserted in response to an external clock, however, stems from the multiplexed bus limitation.

Although it appears that address, data and control information must be asserted in response to an external clock in order to work with the described bus architecture, nothing in the specification expressly requires it. As with the term "bus," here "none of Rambus's statements constitute a clear disclaimer or disavowal of claim scope." *Infineon II*, 318 F.3d at 1095. Without a clear disclaimer in the specification, Rambus's attempt to narrow "synchronous memory device" based on references to a multiplexed bus in the specification is not persuasive.

e. Subsequent briefing

During the claim construction hearing, and in light of the original briefing, the court proposed the construction: "a memory device that receives an external clock to govern the response timing of the memory device's operation(s)." Hynix notes that **[*31]** such a construction would cover devices in which the timing of data input and output is governed by an external

clock, and finds the construction acceptable. Pl.'s Supp. Memo re: "Synchronous Memory Device" and "Packet" at 2. Rambus also finds the court's tentative construction acceptable if the words "response timing" are replaced by the phrase "the timing of input and output operations" to clarify that input and output timings must both be governed by an external clock. Def.'s Supp. Memo re: "Synchronous Memory Device" and "Packet" at 1. Although the parties agree that the specification discloses a preferred embodiment in which both inputs and outputs are governed by an external clock, as discussed earlier, it appears from the claims that Rambus's construction is too narrow. The court finds that the language of the claim supports the definition of "synchronous memory device" as "a memory device that receives an external clock signal which governs the timing of the response to a transaction request."

4. Operation Code

a. Proposed constructions

The disputed term "operation code" is used in U.S. Patent Nos. 6,378,120 ("the '120 patent"), 6,378,020 ("the '020 patent"), **[*32]** 6,426,916 ("the '916 patent"), and 6,452,863 ("the '863 patent"). Rambus proposes that "operation code" be construed as "one or more bits to specify a type of action." Joint Claim Construction Statement ("JCCS") Ex. A at 8. Hynix submits that the term means "bits in a field within a packet or computer code instruction that identifies what type of action to be performed." *Id.* The dispute focuses on Hynix's attempt to limit the operation code to require that the action be performed "within a packet" or "within a computer code instruction." Hynix further objects that Rambus's proposed construction improperly broadens the scope of what could constitute an operation code.

b. Claim language

The claims teach that there are conceptually three types of operation codes. "The first operation code instructs the memory device to perform a read operation." '120 patent, cl. 1. "The second operation code instructs the memory device to perform a write operation." '120 patent, cl. 2. "The third operation code instructs the memory device to store the value [which is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs the data] **[*33]** in a programmable register on the memory device." '120 patent, cl. 12.

The dependent claims recite various properties the operation code may have. "The first operation code [may] n12 include[] precharge information." '120 patent, cl. 7 (which is dependent on claim 1). "The first operation code [may be] included in a request packet." '120 patent, cl. 8 (which is dependent on claim 1). "The block size information and the first operation code [may be] both included in the same request packet." '120 patent, cl. 9 (which is dependent on claim 1). This request packet may also include address information. '120 patent, cl. 10 (which is dependent on claim 8). Finally, the operation codes are issued by a memory controller ('863 patent, cls. 1, 3) and provided to the memory device via an external bus ('120 patent, cl. 21, dependent on cl. 15).

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n12 Throughout this paragraph "may" is inserted because these are dependent claims.

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Hynix argues that "operation code" should be limited to a field within a packet. n13

The **[*34]** context in which the claims use "operation code" does not suggest such a limitation was intended. Claim 1 of the '120 patent (which is asserted), refers to an "operation code" that "instructs the memory device to perform a read operation." Yet, Claim 8 of the '120 patent (which is dependent on Claim 1, but not asserted) specifies that the "operation code is included in a request packet." Claim 24 of the '863 patent (which is dependent upon Claim 14, but is not asserted) also specifies "the operation code, the first block size information and address information are included in a packet." *See* '020 patent, cl. 34 (which is dependent on cl. 32).

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n13 Hynix offers no specific explanation why "operation code" should be limited to fields within a "computer code instruction." Moreover, Hynix proffers no definition for a "computer code instruction." The patents use the term "computer" inconsistently, sometimes referring to a computer as a higher level or simply different device from the present invention. Therefore, Hynix has presented no persuasive evidence demonstrating that the limitation "within a computer code instruction" applies to "operation code."

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The Federal Circuit faced a similar construction issue in *Infineon II*. 318 F.3d at 1095. There, the court reasoned that by claiming a "bus carrying device-select information without the need for separate device-select lines connected directly to individual semiconductor devices" (i.e. a bus *that is* multiplexed), Rambus showed it "did not redefine bus' in the specification to be a multiplexing bus." *Id.* Similarly, by specifying in certain dependent claims that the operation code is included in "a request packet," or simply "a packet," Rambus does not appear to limit "operation code" as used in other claims to bits in a field within a packet.

c. Ordinary meaning

The court looks to the relevant technical dictionaries to ascertain the ordinary and customary meaning of "operation code." *Tex. Digital*, 308 F.3d at 1202. The patents relevant to operation code were issued in 2001 and 2002, so the court looks to the 2001 edition of The Authoritative Dictionary of IEEE Standard Terms for guidance. "Operation code" has the following definition:

> (1)(B) The code that represents or describes a specific operation. The operation code is usually **[*36]** the operation part of the instruction.

THE AUTHORITATIVE DICTIONARY OF IEEE STANDARD TERMS 769 (2001 ed.).

In light of the evidence presented, the court finds this definition to be the ordinary meaning of "operation code." Rambus's proposed construction is substantially similar to this definition, and therefore comports with the ordinary meaning of "operation code." Notably, the ordinary meaning of "operation code" does not connote that it be transmitted solely within a packet.

d. Specification

To rebut the presumption that one skilled in the art would have understood "operation code" to carry its ordinary meaning, Hynix argues the specification defined the claim term by implication to include the packet limitation. *See* Bell Atl. Network Servs. v. Covad Communications Group, Inc., 262 F.3d 1258, 1271 (Fed. Cir. 2001) HN7 ("when a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term by implication'"). Hynix observes that the sole support for the meaning of "operation code" in the specification is in the AccessType field in the preferred embodiment of the request **[*37]** packet.

In the preferred implementation, the operation code is part of the control information. '120 patent, cl. 9, 11. 39-41. The control information is contained within two 4 bit fields that constitute the first byte of a six byte request packet. '120 patent, cl. 9, 1. 25; Fig. 4. The preferred implementation labels the operation code in this packet "AccessType" ('120 patent, cl. 9, 1. 35), which is depicted in Figure 4. AccessType is also depicted in additional types of packets in Figure 5 and Figure 6. The specification explains that AccessType is a field which "specifies whether the requested operation is a read or write and the type of access, for example whether it is to the control registers or other parts of the device, such as memory." '120 patent, cl. 9, 11. 43-46.

In *Toro Co. v. White Consolidated Industries, Inc.*, the Federal Circuit explained that HN8 a limitation upon a claim term may be implied from its existence in the sole preferred embodiment when "no other broader concept was described as embodying the applicant's invention, or shown in any of the drawings, or presented for examination." 199 F.3d 1295, 1301 (Fed. Cir. 1999). The court construed "including" **[*38]** and "cover" as requiring that a restriction ring be permanently attached to the cover because "nowhere in the specification, including its twenty-one drawings, is the cover shown without the restriction ring attached to it" *Id.* Moreover, "the specification described the advantages of the unitary structure as important to the invention." *Id.* Hynix concludes that since the sole use of "operation code" in the preferred implementation is as the AccessType field within a packet, the specification clearly implies that the construction of "operation code" should be limited to being within a packet. *See* Toro, 199 F.3d at 1301.

A weakness in Hynix's position is revealed when the preferred embodiment is viewed in light of *Infineon II.* 318 F.3d at 1095. The Federal Circuit held that Rambus's invention's use of a bus "is not limited to a multiplexing bus." *Id.* Stated another way, the scope of Rambus's invention includes operation on a non-multiplexed bus. The *Infineon II* court defined "multiplexing" as "the sharing of a single set of lines to send multiple types of information," such as address, data and control information. *Id.* at 1094. **[*39]** The preferred embodiment of AccessType being within a request packet is illustrated in Figure 4. The packet depicted in Figure 4 (as well as in Figures 5 and 6) requires the use of a multiplexed bus. For example, in Figure 4, the bus line carrying Access Type[0] would carry the first bit of the operation code on cycle 0, then the same bus line would carry address information on the remaining cycles. The packet depicted in Figure 6 requires the same bus line to carry control information (*i.e.*, AccessType), address information, invalid request information, and request information over the course of 12 bus cycles. The critical fact is that these packets travel on a multiplexed bus and cannot operate on a non-multiplexed bus.

If the preferred embodiment of operation code requires the use of a multiplexed bus, but the Federal Circuit has found the invention may be operated on non-multiplexed bus, then the logical conclusion is that this cannot be the only possible embodiment of the "operation code." *See* SRI Int.'l v. Matsushita Electric Corp., 775 F.2d 1107, 1121 (Fed. Cir. 1985) HN9 (the law does not require an applicant describe in the specification "every conceivable **[*40]** and possible future embodiment of his invention."). Consequently, Rambus's patents are distinguishable from the patents in *Toro. See* 199 F.3d at 1301. In implying a limitation from the preferred embodiment in *Toro*, the court found that "this is not a case of limiting the

claims to a preferred embodiment' of an invention that has been more broadly disclosed." *Id.* In contrast, here the Federal Circuit has found that a broader invention has been disclosed, one in which the claims cover operation on both multiplexed buses and non-multiplexed buses. *Infineon II*, 318 F.3d at 1095. Therefore, a limitation absent in the claims or ordinary meaning of "operation code" cannot be inferred from a preferred embodiment that does not describe the full scope of the claimed invention's method of operation. *See RF Del., Inc. v. Pac. Keystone Techs., Inc.*, 326 F.3d 1255, 1264 (Fed. Cir. 2003) (independent claims usually cover a scope broader than the preferred embodiment, especially when the dependent claims recite the precise scope of the preferred embodiment).

e. Prosecution history

Hynix's citation to Rambus's statements in the prosecution **[*41]** history of the '916 patent is similarly unavailing. Rambus's statements do not add any more context to the definition of "operation code" than what is disclosed in the specification.

f. Breadth

Hynix argues Rambus's definition of "operation code" improperly broadens the term to the point that "any input electrical signal with two possible voltage levels, for example, could qualify as an operation code' as long as some action (on' or off') occurred in response." Hynix's Resp. CC Br. at 17. At first blush, this argument has some appeal. However, the claims themselves limit the practical effect of Rambus's proposed construction. For example, the theoretical input electrical signal that Hynix fears will be considered an operation code still must either "instruct the memory device to perform a read operation," ('120 patent, cl. 1), a "write operation" ('120 patent, cl. 2), or "to store the value in a programmable register on the memory device." ('120 patent, cl. 12). It must also be sampled synchronously with respect to the external clock signal. *Id.* Finally, it must include precharge information. n14 However, only certain claims, like dependent claim 8 of the '120 patent, **[*42]** require that the operation code be contained within a request packet.

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n14 At the least the first such input signal would have to include this information.

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The court is satisfied that Rambus's construction sufficiently "assigns a fixed, unambiguous, legally operative meaning to the claim." *Liquid Dynamics Corp. v. Vaughan Co., Inc.*, 355 F.3d 1361, 1367 (Fed. Cir. 2004). The claim language, the specification, and the prosecution history do not suggest that the patent uses "operation code" in a manner inconsistent with its ordinary meaning. Therefore, the court finds "operation code" is properly construed as "one or more bits to specify a type of action."

5. Block Size Information

a. Proposed constructions

The disputed term "block size information" is used in U.S. Patent Nos. 6,032,214 ("the '214 patent") and 6,034,918 ("the '918 patent") and the '120 and '863 patents. Rambus proposes the term be construed as "[a] value representative of a quantity of data to be transferred during **[*43]** a memory read or write operation." JCCS, App. A at 11. Hynix proposes, "information that specifies the total amount of data that is to be transferred on the bus in response to a [transaction] request." *Id.* The dispute focuses on the amount of data to which

the term refers.

b. Claim language

"In Rambus's invention, the user can specify the amount of data to be transferred over the bus during a bus transaction. This value is represented by the term block size [information].'" *Infineon I*, 2001 U.S. Dist. LEXIS 10990, 2001 WL 34138091 at *16. The claims state that "first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request." '918 patent, cl. 18. The memory device receives the first block size information and responds by "outputting the first amount of data corresponding to the first block size information." *Id.* Similarly, second block size information typically corresponds to the amount of data to be input in response to a second transaction request. '918 patent, cl. 3.

c. Interpretation

Rambus's first objection to Hynix's proposed construction is that it can be interpreted as requiring the value **[*44]** of "block size information" to be equal to the amount of data to be transferred. If this were the case, for example, then when a request called for 1024 bits of data, the value that conveyed block size information would also have to be 1024. Hynix has allayed these fears by pointing out that "the term specify' [in its proposed construction] only indicates that the block size information' is a code that represents the total size of the block of data to be transferred." Hynix at 20; *see also* Reply at 8 n.2. Hynix also notes that "Rambus's construction is ambiguous in failing to specify that the "block size information' defines a single block of data to be transferred in a single device access. Hynix's proposed construction does not contain this ambiguity and is consistent with the specification." Opp. at 19.

The court finds that block size information must be a value that corresponds to the total number of bits to be transferred. Such a construction comports with the construction of the term by the Eastern District of Virginia and is supported by the claims and the specification. *Infineon I*, 2001 U.S. Dist. LEXIS 10990, 2001 WL 34138091 at *17 (construing "block size" as "information that **[*45]** specifies the total amount of data that is to be transferred on the bus in response to a transaction request").

Rambus also seeks to clarify in its reply brief that the "total amount" referred to in "block size information" is the data to be transferred from a single device, not from every memory device in a system. Despite Rambus's fear, nothing in the claims, the specification, or Hynix's arguments suggests that "block size information" relates to the amount of data to be transferred from every memory device in a system. Thus, although the court agrees that the intrinsic evidence supports the position that "block size information" relates only to the amount of data to be transferred from a single device, the court does not agree that Hynix's proposed construction is susceptible to the interpretation that "block size information" refers to the amount of data to be transferred from every memory device in a system. "Block size information" is construed as "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request."

6. Precharge Information

a. Proposed constructions

The disputed term "precharge information" **[*46]** is used in the '120 and '916 patents. Hynix proposes that "precharge information" be construed as "information denoting whether a memory array (or portion of a memory array) should be precharged." JCCS, Ex. A at 13. Rambus proposes a "value that is related to an establishment of a pre-defined voltage state." *Id.*

Originally, Rambus challenged Hynix's definition on the grounds that precharging relates to the sense amps, which would be excluded from Hynix's definition because the sense amps are not part of the memory array. At the hearing, Hynix agreed that "memory array" could be replaced in their proposed construction with "sense amplifiers and bit lines." Tr. 106:1-7. Therefore, Hynix's amended construction of precharge information is "information denoting whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bit lines) should be precharged." Tr. 104:22-24. n15 In light of Hynix's amendment, the only dispute is whether precharge information is simply "related to [the] establishment of a pre-defined voltage state" or more specifically denotes whether the sense amps and bitlines "should be precharged."

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n15 Hynix uses the "or" construction.

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Hynix objects that Rambus's proposed construction of precharge information is devoid of meaning or connection to the use of precharging in the memory device. This objection is well taken. Construing "precharge information" as simply "a value that is related to an establishment of a pre-defined voltage state" imparts no meaningful guidance as to what the term means. *Bell Atl.*, 262 F.3d at 1270 ("ordinary meaning of the non-technical term mode' is sufficiently broad and amorphous that the scope of the claim can be reconciled only with recourse to the written description").

b. Claim language

Before or after each read or write operation at a new address, two components of a DRAM must be precharged, "the bitlines in the [memory] array and the sense amplifiers." Taylor Decl. P 87; *see also* JCCS, Ex. F (JOHN Y. CHEN, CMOS DEVICES AND TECHNOLOGY FOR VLSI 115 (1990)). All of the asserted claims containing the precharge information limitation, in both patents, are identical. They state:

> The method of claim 1 wherein the first operation code includes precharge information. n16

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n16 In all cases, the claim containing "precharge information" is a dependent claim. In the '120 patent claim 7 contains the limitation and is dependent on claim 1. In the '120 patent claim 33 contains "precharge information" and is dependent upon claim 29. In the '916 patent claim 9 contains the limitation and is dependent upon claim 1.

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This claim language by itself does not provide clear meaning. It does, however, provide an important contextual backdrop. The plain meaning of the term shows it must convey

information related to precharging. The claim teaches that the precharge information is included in the first operation code, which means the information is conveyed as part of a command. This implies the precharge information is connected to instructing the device (or a portion of the device) to perform an action. *See supra* (construction of operation code).

c. Specification

Rambus's proposed construction does not include a connection between the act of precharging and a specific component of the memory device. The context in which "precharge" is used in the specification consistently implies such a connection is necessary. Each time the specification discusses precharging it is in connection with a component of the device. More importantly, the specification teaches the precharge information contained in the operation code is used to determine the access mode. The access mode, in turn, "determines whether the DRAM should precharge the sense amplifiers or should save the contents of the sense amps for **[*49]** a subsequent page mode access." '263 patent, cl. 10, 11. 8-14.

Thus, the precharge information does not simply convey a value representing the establishment of a pre-defined voltage state. Instead it conveys whether the device should precharge the "sense amps (and hence the bit lines)" ('263 patent, cl. 10. 1. 43), or not precharge the sense amps so that they can retain the data to be sensed on the next read ('263 patent, cl. 10, 11. 25-30). The parties do not dispute what the specification means by "precharge." Therefore, the court finds that the specification implies "precharge information" as information relating specifically to whether or not a component of the device should be precharged. n17 Rambus's definition does not contain this necessary connection between precharging and specific components of the device. Consequently, "precharge information" is construed as "information denoting whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bit lines) should be precharged."

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n17 As discussed, the parties have agreed that the this component of the device is actually the sense amps and/or the bit lines.

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7. Access Time/ Access Time Register/ Delay Time

a. Proposed constructions

To optimize transmissions over the bus, the invention attempts to coordinate individual DRAM outputs by injecting a certain time delay before each device responds to a request. A value representing the amount of time the device is to delay is stored in one or more access time registers on each device.

Rambus and Hynix dispute the construction of three related terms: (1) access time register, (2) access time; and (3) delay time. These terms are conceptually interrelated which requires they be construed jointly. "Access time register" is used in '214 patent, claim 18 and the '918 patent, claim 24. The parties have agreed to the construction of "register" as "a data storage element or group of data storage elements not part of a memory array that can store one or more bits of information." Rambus proposes "access time register" be construed as "[a] data storage element to store a value representative of an access time delay." Hynix proposes it be construed as "[a] register programmable to store information representing a particular access time." JCCS, Ex. A at 24.

"Access time" is used throughout **[*51]** the patents yet never as a separate term in the asserted claims. Hynix argues the term should be separately construed by the court because the parties have agreed to a construction of "register," and because both parties use the term in their proposed constructions of several other terms. Hynix proposes "access time" be construed as "the time between the initiation of a memory access and the availability of data at the outputs." JCCS, Ex. A at 22. Rambus opposes a construction of "access time" because the term is only used within the asserted claims as part of "access time register." Although Rambus's briefing contains several arguments in opposition to Hynix's proposed definition, Rambus does not provide a proposed construction for "access time." JCCS, Ex. A at 22.

"Delay time" is used in the '263, '918, '365, and '195 patents. Hynix proposes the term be construed as "the time between the initiation of a memory access and the availability of data at the outputs." JCCS, Ex. A at 25. Rambus proposes "an amount of time before commencing a subsequent action." *Id.*

b. Access Time Register

i. Claim Language

Two asserted claims use the term "access time register." Each **[*52]** provides significant context for construing the term. Claim 18 of the '214 patent states:

> The method of claim 15 [describing the read and output of data synchronously with respect to a first and second external clock signal] further including storing a code in an access time register, the code being representative of a number of clock cycles of the first and second external clock signals to transpire before data is output onto the bus in response to the first read request, wherein the first amount of data corresponding to the first block size information is output after the number of clock cycles transpire.

Claim 24 of the '918 patent states:

> The method of claim 18 [describing the read and output of data synchronously with respect to the external clock signal] further including storing a delay time code in an access time register, the delay time code being representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request and wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time code.

Throughout the patents-in-suit various **[*53]** phrases are used to describe what the value in the "access time register" is meant to represent. Hynix offers "a particular access time." Rambus offers "an access time delay." For puposes of this subsection, in an effort to avoid confusion, the court will use the term "delay time code." n18

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n18 This is not to be interpreted interchangeably with the disputed term "delay time."

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ii. Ordinary meaning

Hynix argues that the contents of the access time register should be defined as a value representing a time equivalent to the ordinary meaning of "access time." The ordinary meaning of "access time" is "the time interval between the instant at which data are called for from a storage device and the instant delivery is completed, that is, the read time." THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 7 (7th ed. 2001). Hynix's proposed construction of "access time" is substantially similar to its ordinary meaning.

Rambus contends that the claims asserted use the term "access time" as simply a label for that **[*54]** type of register. The label, according to Rambus, does not thereby define the contents of the register. The claims' explicit statement that the access time register stores a delay time code supports Rambus's argument. Delay time, as discussed below, is not necessarily equal to Hynix's construction of "access time." Therefore, the ordinary meaning of the label "access time register" does not control the construction of its contents.

iii. Specification

Hynix seeks to limit the delay time code to "a particular access time." Hynix further seeks to precisely define how such "access time" is measured. JCCS, Ex. A at 22. Rambus argues the claims should not be limited to registers where the delay time (represented by the delay time code) is equal to the access time as measured by Hynix.

Hynix's construction of "access time" appears to describe the physically minimum access time. As Rambus observes, in one sense, "access time" describes a physical characteristic of the memory device. It is the minimum amount of time in which it is physically possible for a device to receive a request and then complete its response, whether that response be to write a block of data or to output a block **[*55]** of data through the output pins. *See* THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 7 (7th ed. 2001). As noted during the tutorial, the physical access time of a device is typically a fixed constant, predetermined by the access mode, the physics of the chip, and the interaction with external variables such as temperature or voltage.

First, in a preferred embodiment, the specification teaches:

> The value stored in a slave access-time register 173 is preferably one-half the number of bus cycles for which the slave device should wait before using the bus in response to a request.

'263 patent, cl. 15, 11. 57-60. As this passage illustrates, the access time register changes the amount of time in which a memory device returns data depending on the value stored in the register. Murphy Reply Decl. P 25. The critical technical aspect of this concept, that is not

necessarily included in Hynix's proposed construction of "access time," is the injection of a potential and variable delay in the device's response.

Second, the specification reveals that it would be improper to limit the delay time, or the value stored in the access time register, to any single value. The **[*56]** specification states:

> The configuration master should choose and set an access time in each access-time register 173 in each slave to a period sufficiently long to allow the slave to perform an actual, desired memory access. For example, for a normal DRAM access, this time must be longer than the row address strobe (RAS) access time. If this condition is not met, the slave may not deliver the correct data. The value stored in a slave access-time register 173 is preferably one-half the number of bus cycles for which the slave device should wait before using the bus in response to a request. Thus an access time value of 1' would indicate that the slave should not access the bus until at least two cycles after the last byte of the request packet has been received. The value of AccessReg0 is preferably fixed at 8 (cycles) to facilitate access to control registers. '263 patent, cl. 15, 11. 51-65.

Thus, the patent contemplates that the user can set the delay time to any desired value. The preferred embodiment takes steps to teach what the patentee believed to be the optimal delay times for the various access modes. However, the consistent use of terms such as "should," "preferably, **[*57]** " and "choose" demonstrates the user is not required to set the delay time to any fixed or pre-determined value. Therefore, this court will not read such a limitation from the preferred embodiment into the construction of "access time register."

Similarly, it would be improper to limit the measurement of the delay time to ending at any specific pre-defined event. The specification explains:

> [A] slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin *or* possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase.

'263 patent, cl. 8, 11. 39-42 (emph. added).

This passage demonstrates the patent contemplates the possibility that the delay time could be set to end either before or after the completion of a device internal phase. Rambus, however, agreed at the hearing that the time can be limited to commencing when the device receives a transaction request. Tr. 118:21. n19

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n19 In the construction of "access time register" the court adopts below, the court uses the phrase "receiving a transaction request" to describe the starting point of this time delay. To the extent this phrase contains any ambiguity, the court notes that the claims using "access time register" often describe the starting and ending events used to measure this delay time code. The court intends for its construction to be interpreted as a generic term which is further defined by the specific claims at issue. Tr. 117:2-118:4.

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iv. Rambus's construction is ambiguous

Rambus proposes the value in the access time register be construed as representing "access time delay." JCCS, Ex. A at 24. Hynix objects that this construction is circular and ambiguous. Notably, Rambus made similar objections to Hynix's proposed construction of "access time." Those same objections undermine the soundness of using "access time delay" in the construction. Having found that the ordinary meaning of "access time" does not necessarily equal the delay time, the court finds "access time delay" provides little guidance when evaluating possible infringement.

In searching for a clearer way to define the value stored in the access time register, the court finds the specification's description to be accurate and clear. Therefore, "access time register" is construed as "a data storage element to store a value representative of a time a device must wait from receiving a transaction request before responding to a transaction request." Tr. 118:18-20.

c. Delay Time

Hynix proposes "delay time" be construed using the same definition it proposed for "access time." For the reasons discussed in reference to the "access time register, **[*59]** " "delay time" cannot be limited to equaling any fixed access time, nor can it be precisely measured in the fashion Hynix proposes. In addition, Hynix includes in its definition of delay time, "the availability of data at the outputs." Yet, the claims using "delay time" separately already set forth the action that occurs after the delay time expires. For example, claim 1 of the '263 patent involves "a programmable register to store a value which is representative of a delay time after which the memory *responds to a read request*." (emphasis added) Adopting Hynix's construction of delay time would render the representative claim 1's expression of the subsequent action (emphasized in quotation) superfluous.

Since each claim in which "delay time" is used as a separate term (as opposed to "delay time code") provides sufficient context to ascertain the purpose and functionality of the concept, "delay time" shall simply be construed "as an amount of time that must transpire before commencing an action." The court finds this construction to comply most closely with the term's ordinary meaning. *See* OXFORD ENGLISH DICTIONARY (2d ed. 1989).

8. "Value That is Representative of an Amount [*60] of Time to Transpire"/" Value Which is Representative of a Delay Time"/" Value Which is (or Code Being) Representative (or Indicative) of a (Preprogrammed) Number of Clock Cycles"

The parties dispute the following three terms: (1) "value that is representative of amount of time to transpire" used in the '916 patent; (2) "value which is representative of a delay time" used in the '263, '365, and '195 patents; (3) "value which is (or code being) representative (or indicative) of a (preprogrammed) number of clock cycles" used in the '263,'443, '214, '918, '195, '592, '152, '120, and '916 patents. Hynix proposes each of these terms be defined as "information representing a particular access time." JCCS, Ex. A at 26-28. Rambus contends the terms are self-explanatory in light of their context within the claims. Rambus is correct The court finds the patents used these terms in a manner equivalent to delay time code or "delay time." The problems discussed with Hynix's proposed construction of "access time register" and "delay time" apply equally to its construction of these terms.

Accordingly, the court adopts Rambus's proposed construction for each of these terms. Each term is interpreted **[*61]** to represent a value conceptually similar to the delay time code

and "delay time" discussed above. "Value that is representative of amount of time to transpire" is construed as "information that indicates an amount of time which is to occur." JCCS, Ex. A at 26. "Value which is representative of a delay time" is construed as "information which indicates a delay time." *Id.* "Value which is (or code being) representative (or indicative) of a (preprogrammed) number of clock cycles" is construed as "information which indicates a number of clock cycles."

9. Data

In light of the court's refusal to construe "device" as requiring a multiplexed bus, the parties agree that construction of "data" is no longer necessary. (Tr. 107:10-108:11.).

10. Control Information

Since the court does not construe "device" as requiring a multiplexed bus, the parties agree that construction of "control information" is no longer necessary. (Tr. 107:10-108:11.)

11. "First External Clock" and "Second External Clock"

a. Proposed constructions

Hynix contends that "first external clock" should be construed as "a periodic signal received by the memory device from an external source to **[*62]** provide first timing information." *See Infineon I*, 2001 U.S. Dist. LEXIS 10990, 2001 WL 34138091 at *26. Rambus proposes that the term should be construed the same as "external clock signal" -- "a periodic signal from a source external to the device to provide timing information."

Similarly, Hynix contends that "second external clock" should mean "a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information." *See Infineon I*, 2001 U.S. Dist. LEXIS 10990, 2001 WL 34138091 at *26. Rambus, in contrast, proposes second external clock signal to be interpreted as "another external clock signal."

The parties agree that "external clock signal" should be construed as "a periodic signal from a source external to the device to provide timing information." JCCS at 3. They disagree over whether the terms "first" and "second" refer to timing, or whether they refer to two separate signals without reference to time. "Although referred to as a clock' by one skilled in the art, the clock of a memory chip is actually a set of timing information derived from an oscillating reference voltage ("VREF") which cycles between two **[*63]** voltage levels." *Infineon I*, 2001 U.S. Dist. LEXIS 10990, 2001 WL 34138091 at *24. As Rambus claimed in *Infineon I*, Rambus's proposed definitions here "do not require that the two signals contain different timing information," while Hynix's construction requires "that the second signal contain different information from the first." *Id.*

In a July 28, 2003 order, this court vacated in its entirety its previous November 21, 2001 order granting partial summary judgment to Hynix finding, *inter alia*, that "the elements of collateral estoppel are no longer met in this case." Order of 7/25/03 at 3. Besides briefing the collateral estoppel issue extensively, Rambus offers in support of its construction the IEEE Dictionary definitions for "clock" and "signal." *See* JCCS at 17.

To operate the Rambus bus architecture at high speed, "every system, every . . . chip, every component on the bus has to be operating under the exact same timing constraints. That's why it's important and valuable . . . to use a clock design that will synchronize everything together." *Infineon I*, 2001 U.S. Dist. LEXIS 10990, 2001 WL at 34138091 at *26 n.38. Reviewing figures 8A and 8B of the '918 patent, n20 the court first explained **[*64]** that chips N and O were located in different positions along the bus lines, and therefore received

the "clock signals at different points in time due to their locations relative to the origin of the clock signal." 2001 U.S. Dist. LEXIS 10990, [WL] at *25. In order to correct this delay, the memory system reflects a signal along a second line to create a second clock signal, and from these two signals "chips N and O create an internal clock signal which corrects the clock skew caused by propagation delay." *Id.* Notably, Rambus's expert in *Infineon* admitted that in order to correct the skew, the two signals must contain different information. *Id.* The district court went on to note that the only embodiment of the clock in the entire specification required two external signals containing different information in order to create an internal clock, thus correcting the clock skew problem. *See* 2001 U.S. Dist. LEXIS 10990, [WL] at *26.

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n20 U.S. Patent No. 6,034,918. These figures are the same for the '152 and '263 patents.

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Besides introducing evidence from the **[*65]** IEEE Dictionary defining the terms "clock" and "signal," Rambus does not address the *Infineon* district court's analysis. Rambus also fails to suggest an alternative embodiment in the specification under its proposed construction that would address the clock skew problem. HN10 "Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question." *Scimed Life Sys. v. Adv. Cardiovascular Sys.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001); *Watts v. XL Sys., Inc.*, 232 F.3d 877, 883 (Fed. Cir. 2000) (where specification describes only one method to achieve sealing connection, claim limited to that disclosed method); *Toro Co. v. White Consol. Indus.*, 199 F.3d 1295, 1301 (Fed. Cir. 1999) (limiting claims to preferred embodiment, and noting the "specification shows only a structure whereby the restriction ring is part of the cover, in permanent attachment. This is not simply the preferred embodiment; **[*66]** it is the only embodiment.").

The court construes "first external clock" as "a periodic signal received by the memory device from an external source to provide first timing information," and "second external clock" as "a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information."

III. CLAIM CONSTRUCTION

Having considered the papers submitted by the parties and the arguments of counsel during the claim construction hearing, the court interprets the disputed claim terms as set forth below. The disputed claim terms are identified in bold.

CLAIM LANGUAGE	CONSTRUCTION
device	no separate construction
integrated circuit	device a circuit constructed on a single monolithic substrate, commonly called a chip'
synchronous memory device	a memory device that receives an external clock signal which governs the timing of the response to a transaction request
operation code	one or more bits to specify a type of action
block size information	information that specifies the total amount of data

	that is to be transferred on the bus in response to a transaction request
precharge information	information denoting whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bit lines) should be precharged
data	no construction
control information	no construction
synchronized	having a known timing relationship with respect to
first external clock	a periodic signal received by the memory device from an external source to provide first timing information
second external clock	a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information
access time	no separate construction
access time register	a data storage element to store a value representative of a time a device must wait from receiving a transaction request before responding to a transaction request
delay time	an amount of time that must transpire before commencing an action
value that is representative of an amount of time to transpire	information that indicates an amount of time which is to occur
value which is representative of a delay time	information which indicates a delay time
value which is (or code being) representative (or indicative) of a (preprogrammed) number of clock cycles	information which indicates a number of clock cycles
request to provide data	a series of bits used to request a read of data from a memory device where the request identifies what type of read to perform

[*67]

III. ORDER

For the foregoing reasons, IT IS SO ORDERED.

DATED: November 15, 2004

RONALD M. WHYTE

United States District Judge

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